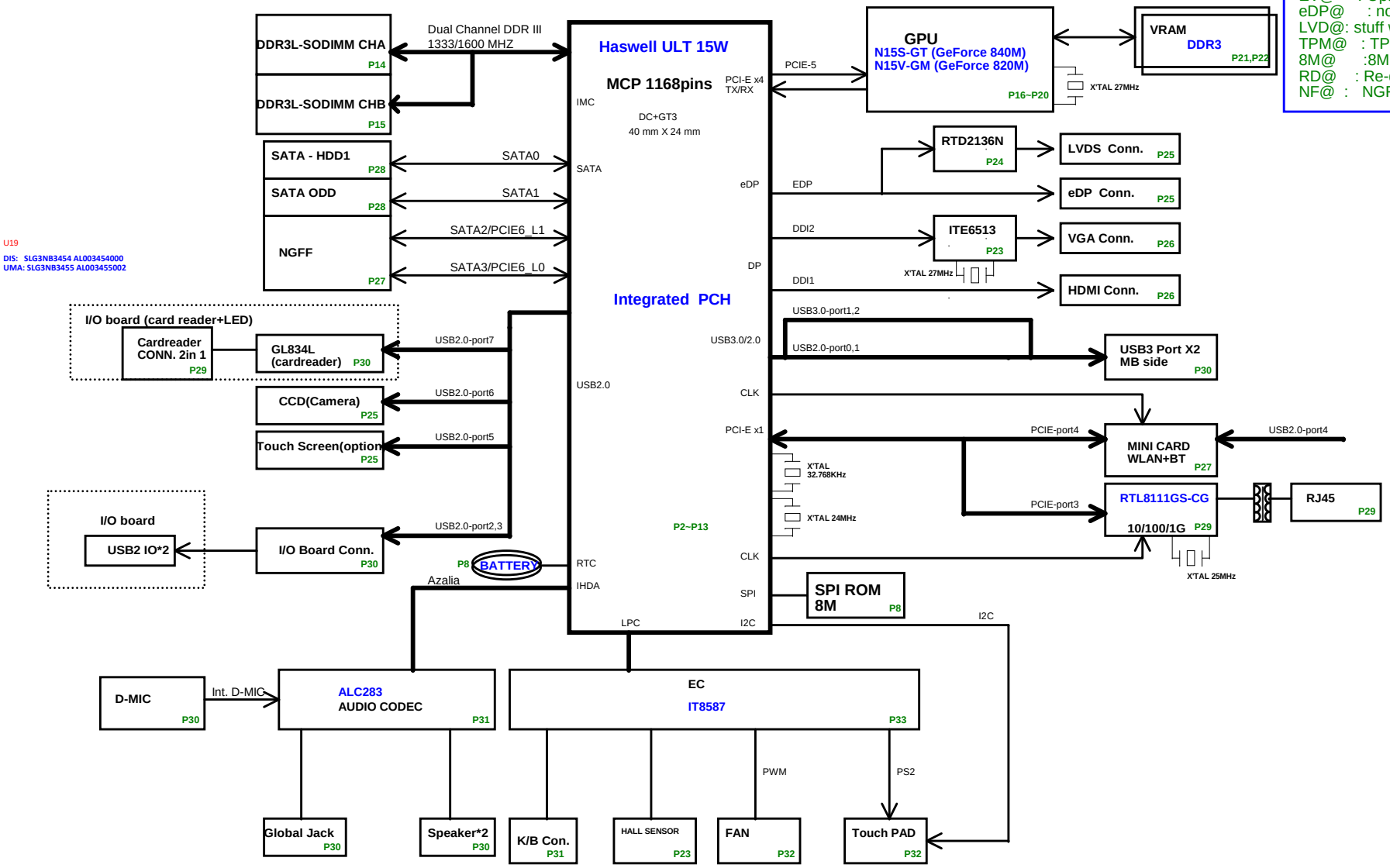
ZYW ULT SYSTEM BLOCK DIAGRAM

01

BOM

IV@ : iGPU
EV@ : Optimus
eDP@ : no stuff when use LVDS
LVD@: stuff when use LVDS
TPM@ : TPM
8M@ :8M FLASH ROM
RD@ : Re-driver SATA
NF@ : NGFF card



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PROJECT : ZYW
Size | Document Number | Rev 3A
Block Diagram
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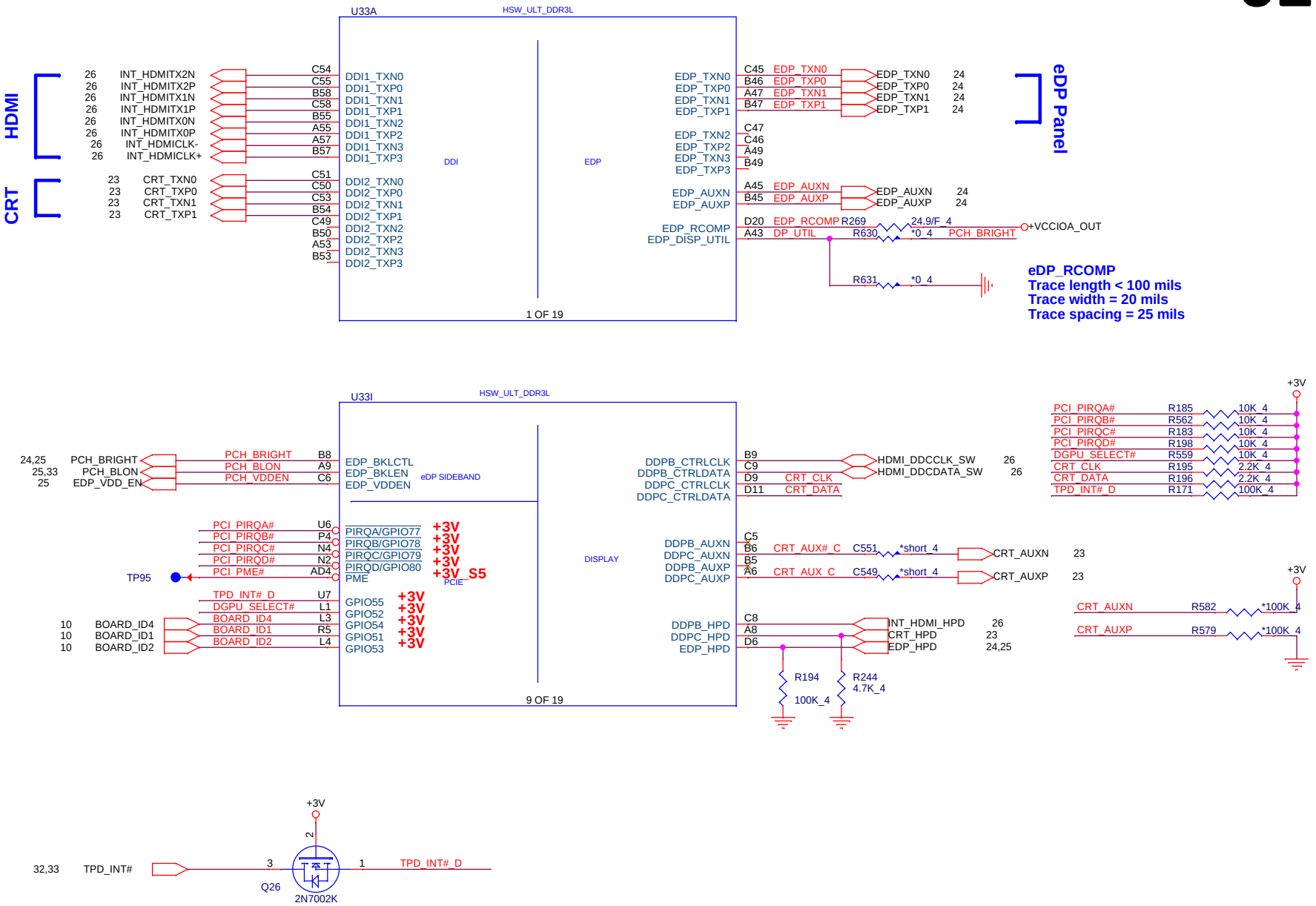
Haswell ULT (DISPLAY,eDP)

02



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PROJECT : ZYW

Size	Document Number	Rev
	Haswell 3/5 (DDI/eDP)	3A

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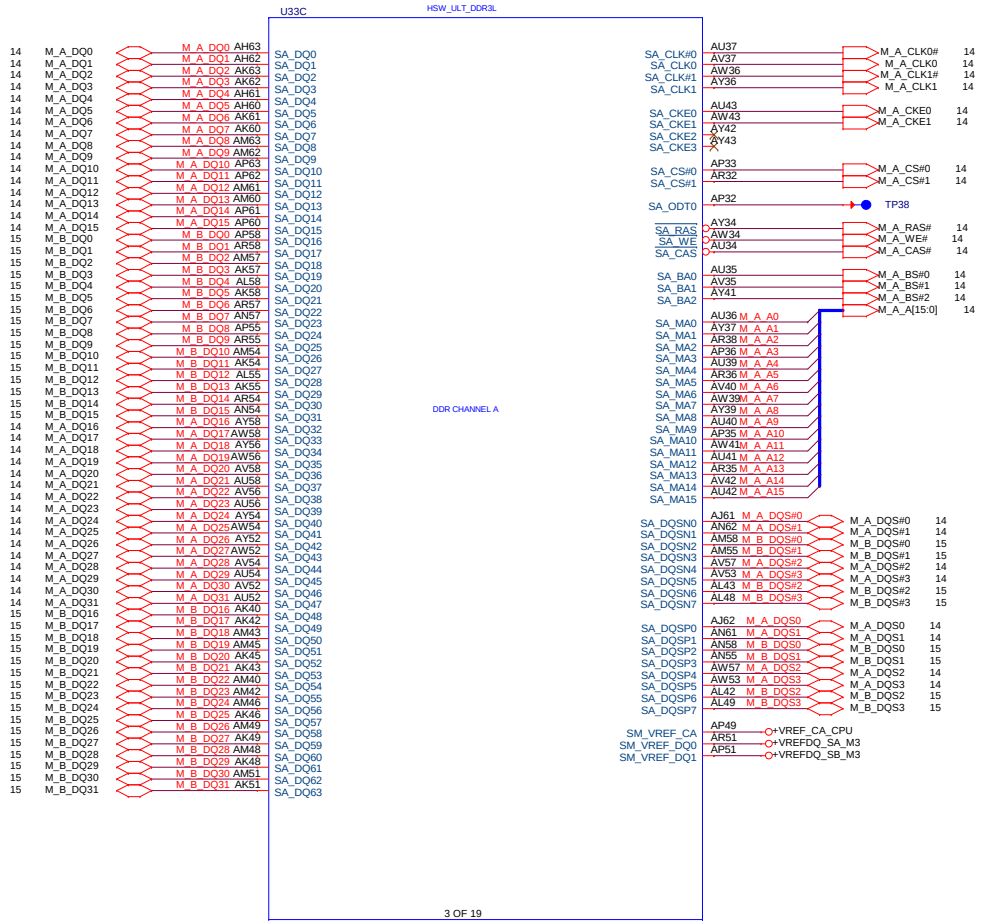
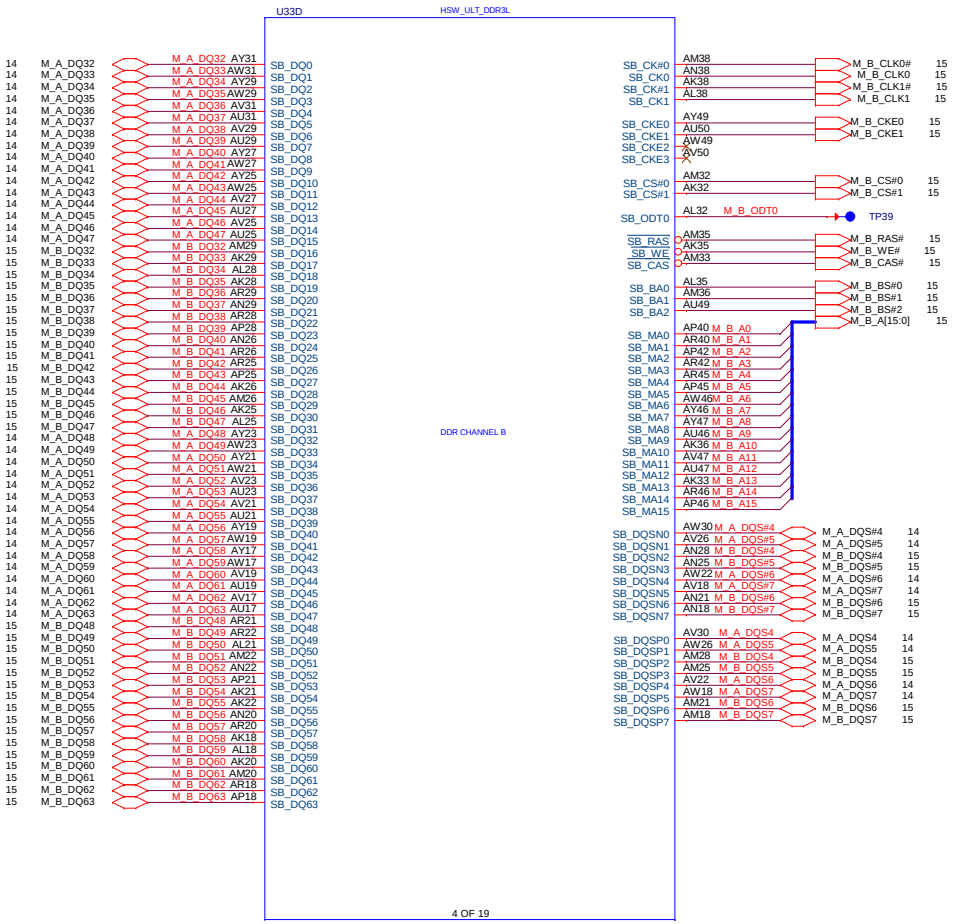
Haswell ULT (DDR3L)



Haswell Processor (DDR3)



03

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PROJECT : ZYW

Size	Document Number	Rev
	Haswell 2/5 (DDR3 I/F)	3A

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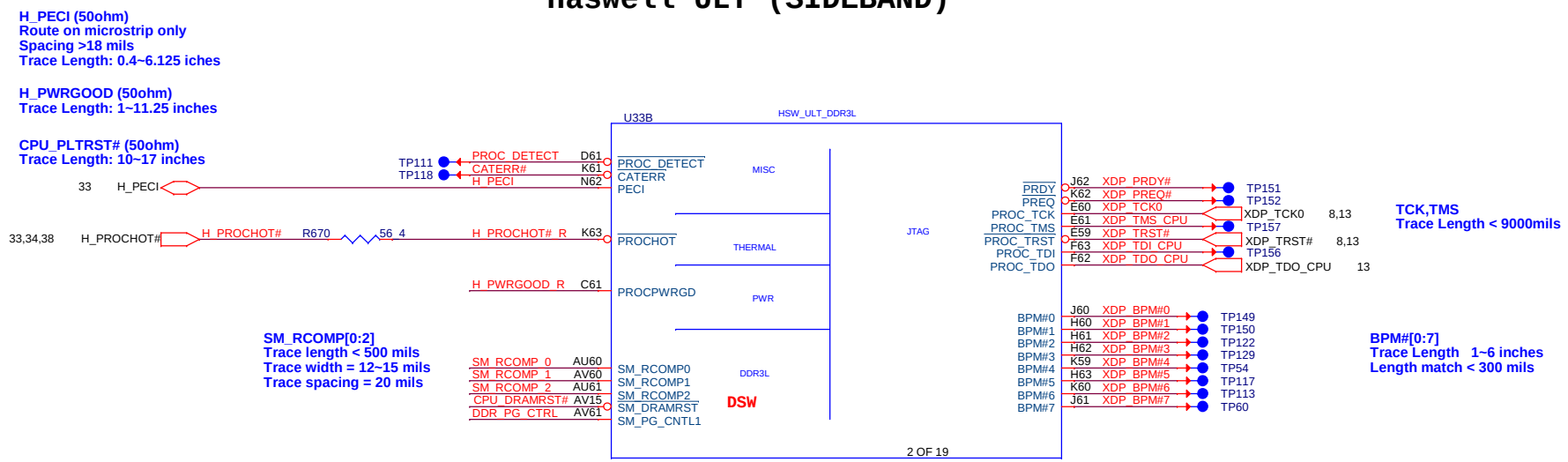
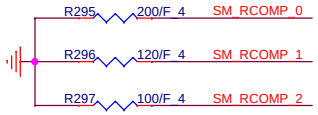
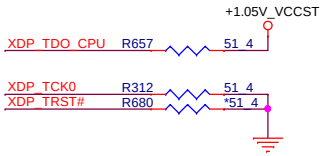
Haswell ULT (SIDEBAND)



DRAM COMP

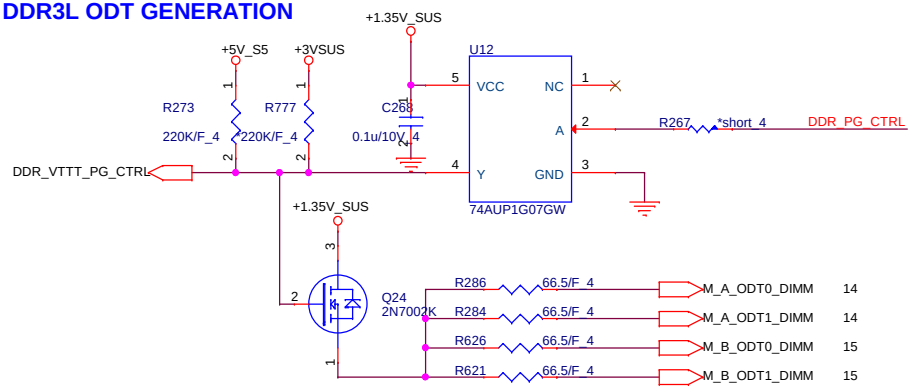


XDP PU/PD

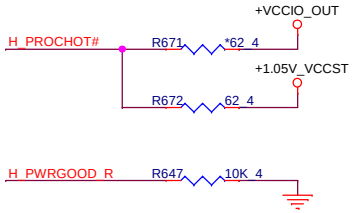


37

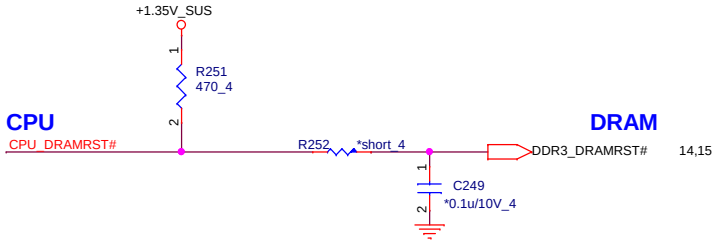
DDR3L ODT GENERATION



PU/PD of CPU



DRAMRST



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	Haswell 1/5 (PEG/DMI/FDI)	3A

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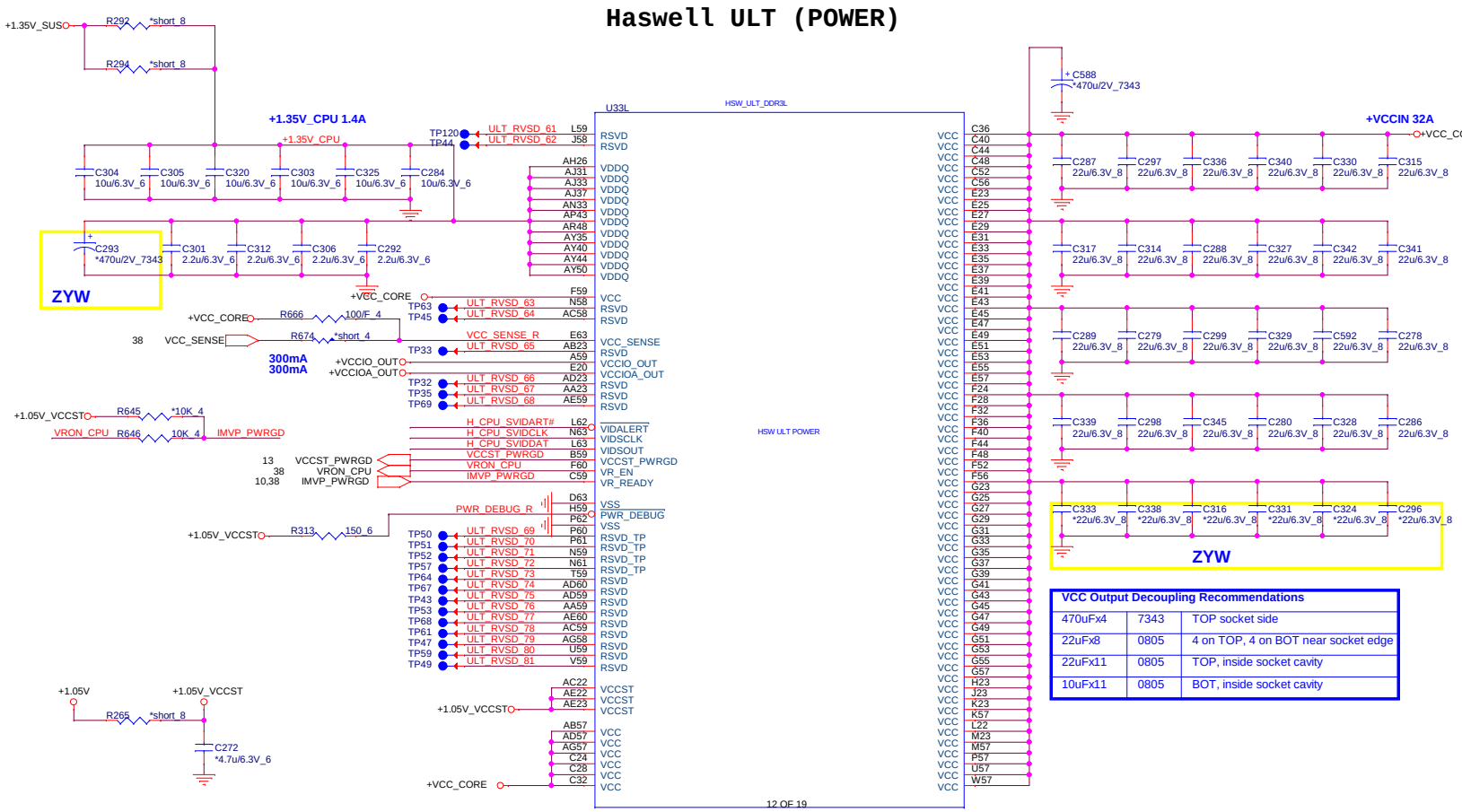
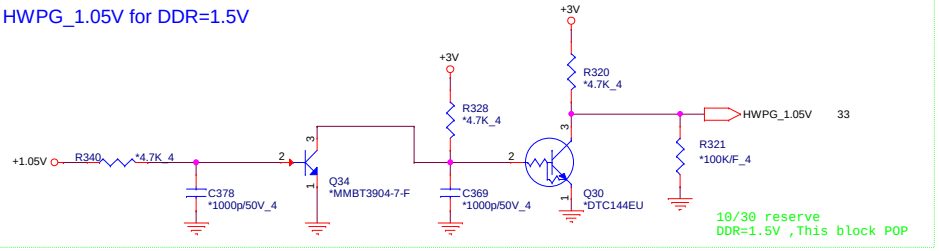
Haswell ULT (POWER)



VCC Output Decoupling Recommendations		
470uFx4	7343	TOP socket side
22uFx8	0805	4 on TOP, 4 on BOT near socket edge
22uFx11	0805	TOP, inside socket cavity
10uFx11	0805	BOT, inside socket cavity

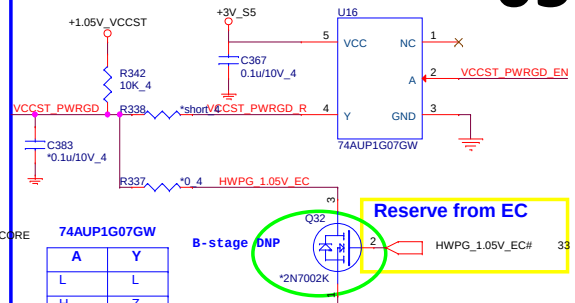
HWPG_1.05V for DDR=1.5V



VCCST PWRGD

CRB is via +1.05V PG

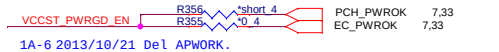
05



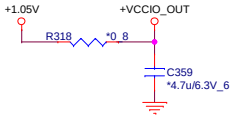
74AUP1G07GW

A	Y
L	L
H	Z

B-stage DNP

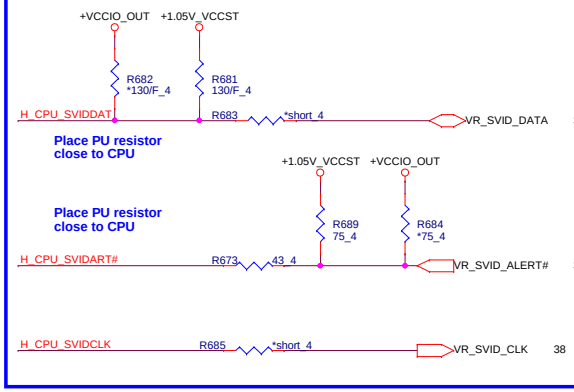


1A-6 2013/10/21 Del APWORK.



SVID

Layout note: need routing together and ALERT need between CLK and DATA.



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PROJECT : ZYW

Size	Document Number	Rev
	Haswell 4/5 (POWER)	3A

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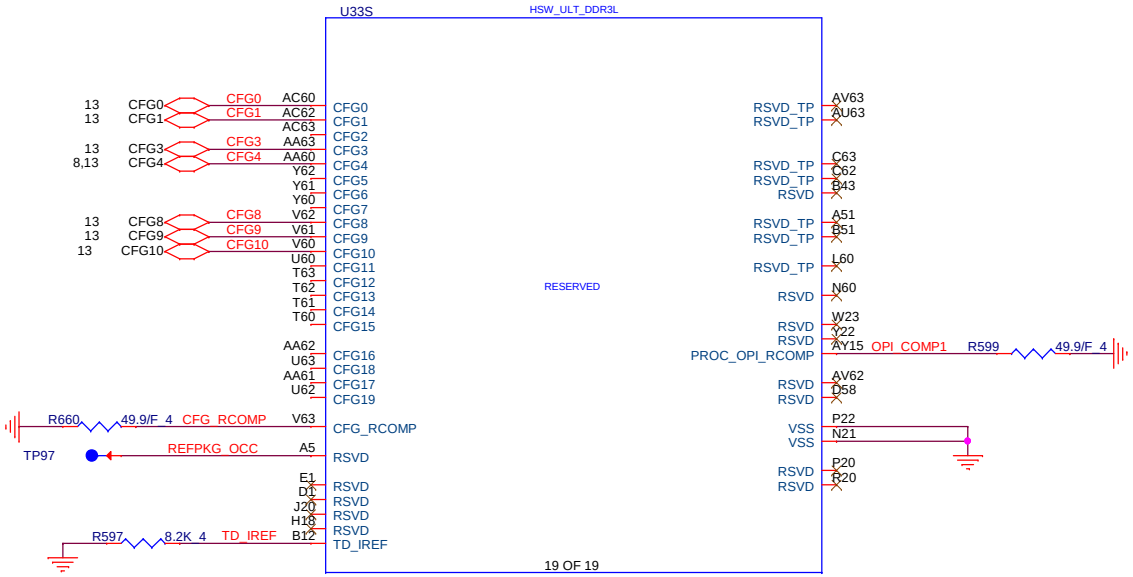
Haswell ULT (CFG,RSVD)

06



Processor Strapping

	1	0	
CFG0 EAR-STALL/NOT STALL RESET SEQUENCE AFTER PCU PLL IS LOCKED	**(DEFAULT) NORMAL OPERATION; NO STALL**	STALL	CFG0 R306 *1K_4
CFG1 PCH/ PCH LESS MODE SELECTION	**(DEFAULT) NORMAL OPERATION**	PCH-LESS MODE	CFG1 R688 *1K_4
CFG3 PHYSICAL_DEBUG_ENABLED (DFX PRIVACY)	**DISABLED NO PHYSICAL DISPLAY PORT ATTACHED TO EMBEDDED DISPLAY PORT**	ENABLED AN EXTERNAL DISPLAY PORT DEVICE IS CONNECTED TO THE EMBEDDED DISPLAY PORT	CFG3 R687 *1K_4
CFG 8 ALLOW THE USE OF NOA ON LOCKED UNITS	**DISABLED(DEFAULT); IN THIS CASE, NOA WILL BE DISABLED IN LOCKED UNITS AND ENABLED IN UN-LOCKED UNITS**	ENABLED; NOA WILL BE AVAILABLE REGARDLESS OF THE LOCKING OF THE UNIT	CFG8 R686 *1K_4
CFG9 NO SVID PROTOCOL CAPABLE VR CONNECTED	**VRS SUPPORTING SVID PROTOCOL ARE PRESENT**	NO VR SUPPORTING SVID IS PRESENT. THE CHIP WILL NOT GENERATE (OR RESPOND TO) SVID ACTIVITY	CFG9 R676 *1K_4
CFG10 SAFE MODE BOOT	**POWER FEATURES ACTIVATED DURING RESET**	POWER FEATURES (ESPECIALLY CLOCK GATINE ARE NOT ACTIVATED	CFG10 R307 *1K_4

Quanta Computer Inc.

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	Haswell 5/5 (CFG/GND)	3A

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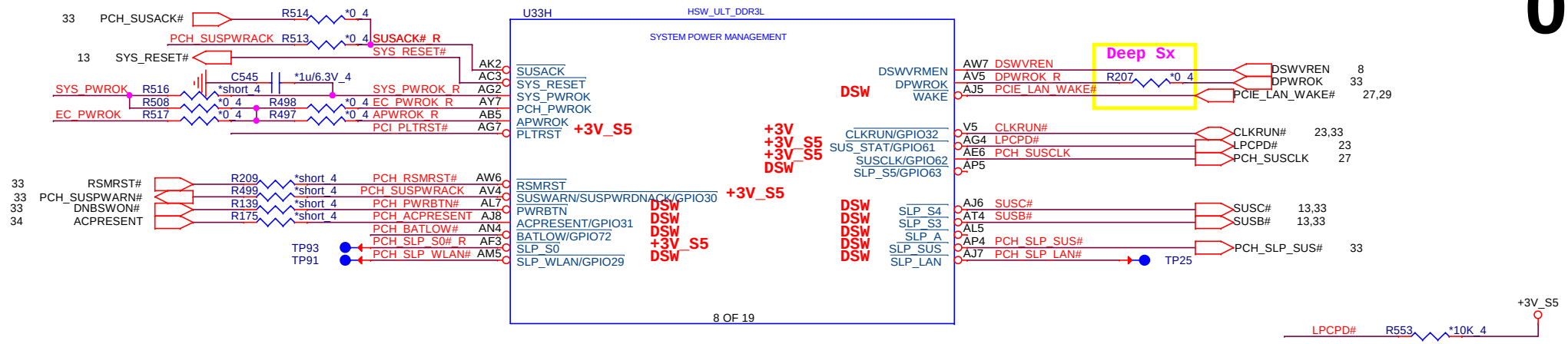
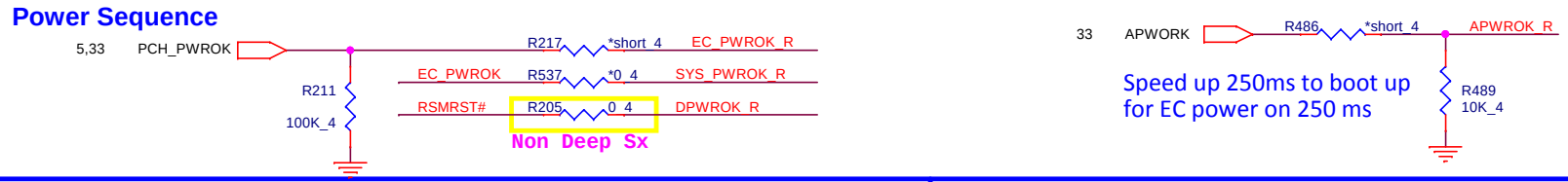
Haswell ULT PCH (PM)

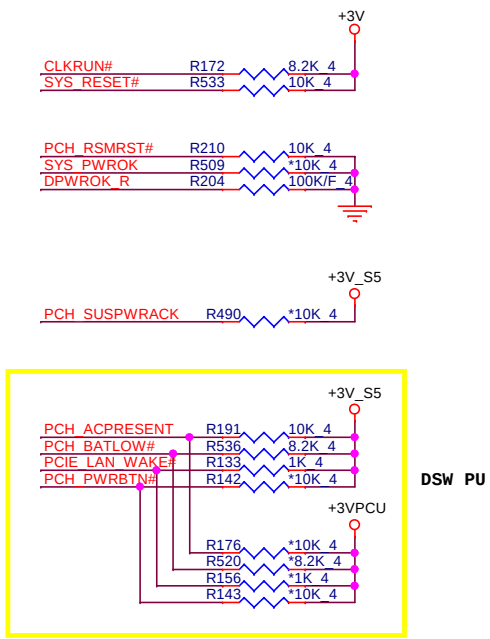
07



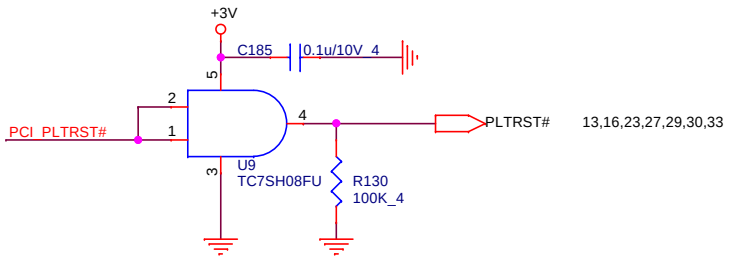
Power Sequence



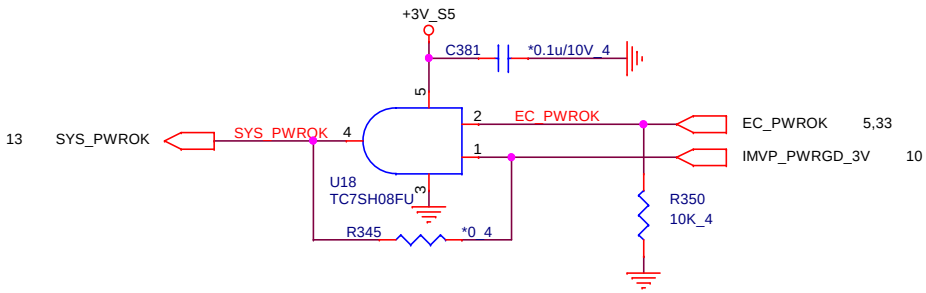
PCH PM PU/PD



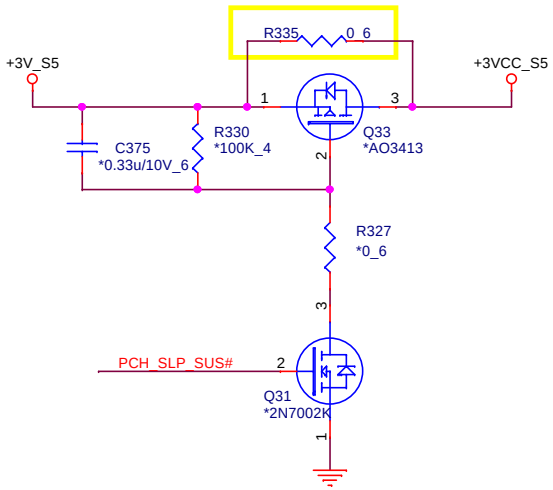
PLTRST# Buffer



SYSPWOK



Deep Sx Circuit



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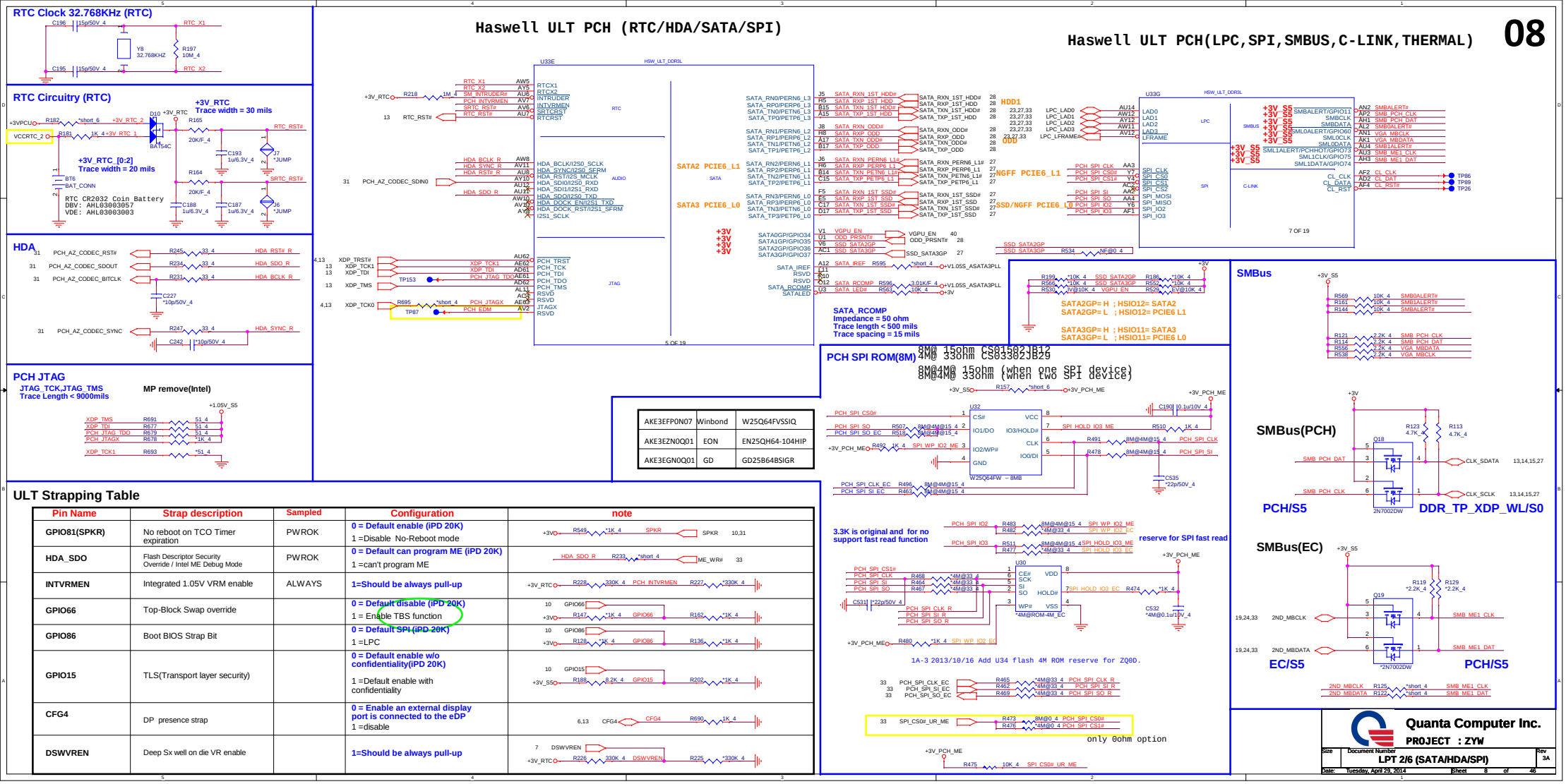
Haswell ULT PCH (RTC/HDA/SATA/SPI)

Haswell ULT PCH(LPC,SPI,SMBUS,C-LINK,THERMAL)



AKE3EFP0N07	Winbond	W25Q64FVSSIQ
AKE3EZN0Q01	EON	EN25QH64-104HIP
AKE3EGN0Q01	GD	GD25B64BSIGR

ULT Strapping Table

Pin Name	Strap description	Sampled	Configuration	note
GPIO81(SPKR)	No reboot on TCO Timer expiration	PWROK	0 = Default enable (iPD 20K) 1 =Disable No-Reboot mode	+3V R549 *1K_4 SPKR SPKR 10,31
HDA_SDO	Flash Descriptor Security Override / Intel ME Debug Mode	PWROK	0 = Default can program ME (iPD 20K) 1 =can't program ME	HDA_SDO_R R233 *short_4 ME_WR# 33
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	1=Should be always pull-up	+3V_RTC R228 330K_4 PCH_INTVRMEN R227 *330K_4
GPIO66	Top-Block Swap override		0 = Default disable (iPD 20K) 1 = Enable TBS function	10 GPIO66 +3V R147 *1K_4 GPIO66 R162 *1K_4
GPIO86	Boot BIOS Strap Bit		0 = Default SPI (iPD 20K) 1 =LPC	10 GPIO86 +3V R128 *1K_4 GPIO86 R136 *1K_4
GPIO15	TLS(Transport layer security)		0 = Default enable w/o confidentiality(iPD 20K) 1 =Default enable with confidentiality	10 GPIO15 +3V_S5 R188 8.2K_4 GPIO15 R202 *1K_4
CFG4	DP presence strap		0 = Enable an external display port is connected to the eDP 1 =disable	6,13 CFG4 CFG4 R690 1K_4
DSWVREN	Deep Sx well on die VR enable		1=Should be always pull-up	7 DSWVREN +3V_RTC R226 330K_4 DSWVREN R225 *330K_4

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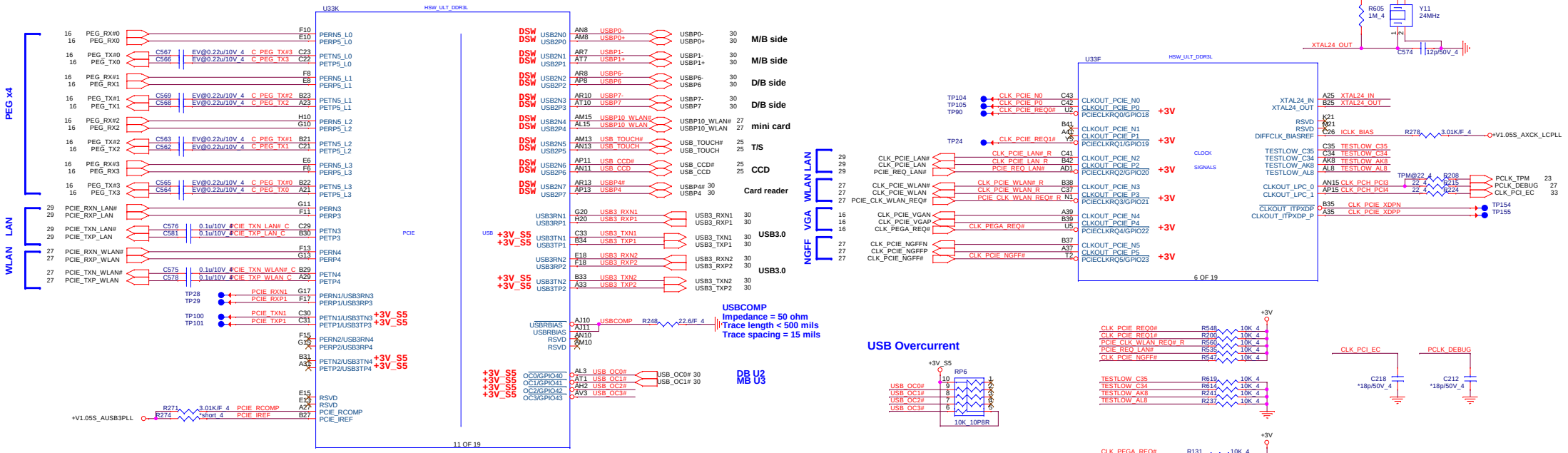
Haswell ULT PCH (PCIE,USB3.0,USB2.0)

Haswell ULT PCH (CLOCK)

09



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PROJECT : ZYW

Size	Document Number	Rev
	LPT 3/6 (PCIE/USB/CLK)	3A

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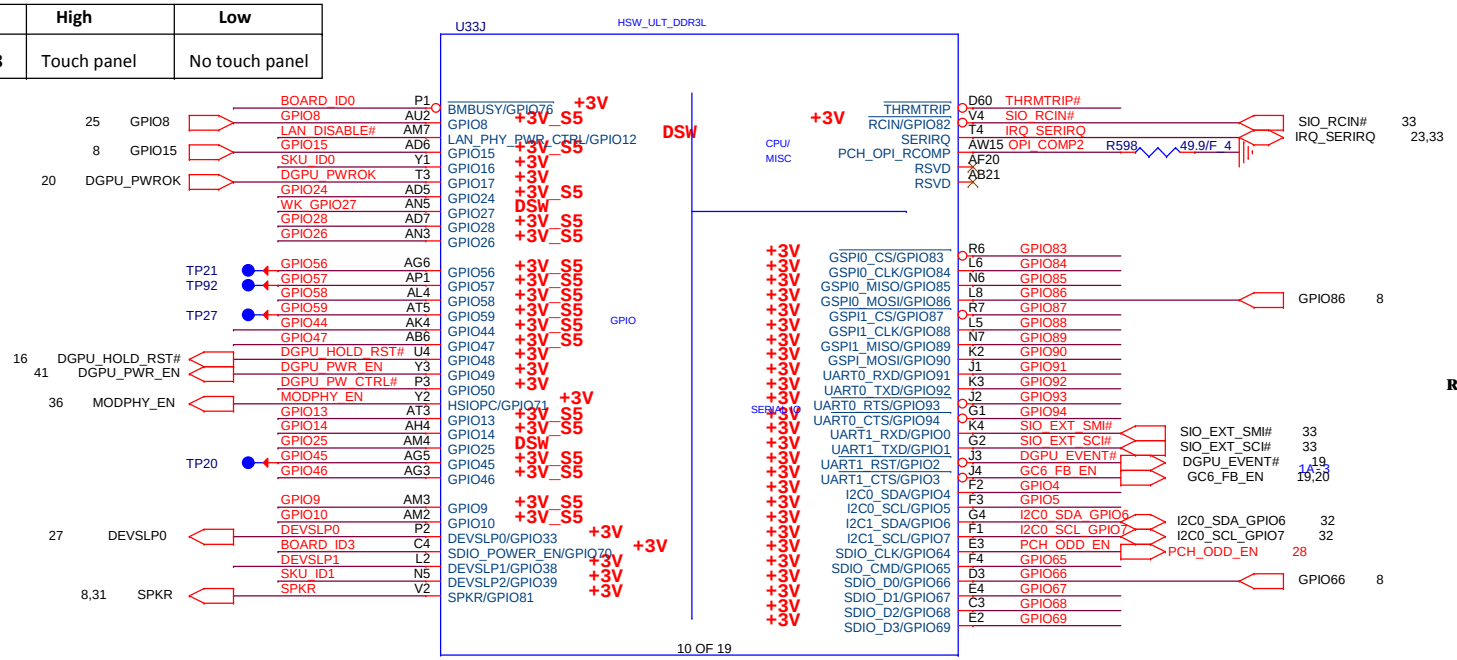
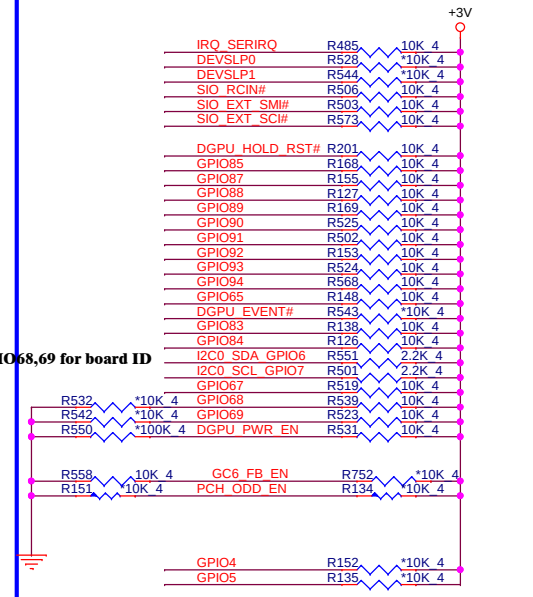
Haswell ULT PCH (GPIO,CPU/MISC,NCTF)

10

	High	Low
GPIO8	Touch panel	No touch panel

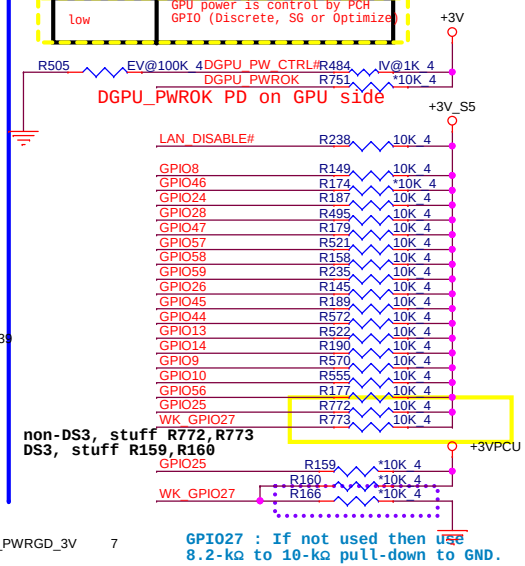


PCH GPIO PU/PD

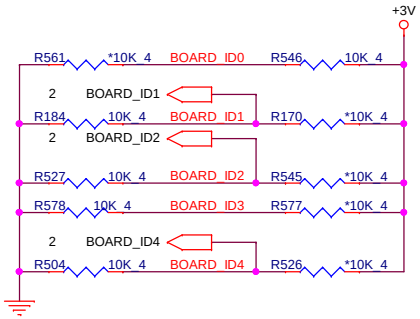


Reserve GPIO68,69 for board ID

high	UMA Only	
low	GPU power is control by PCH GPIO (Discrete, SG or Optimize)	

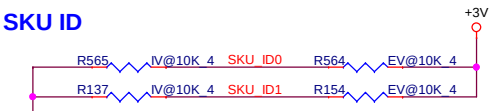


Board ID



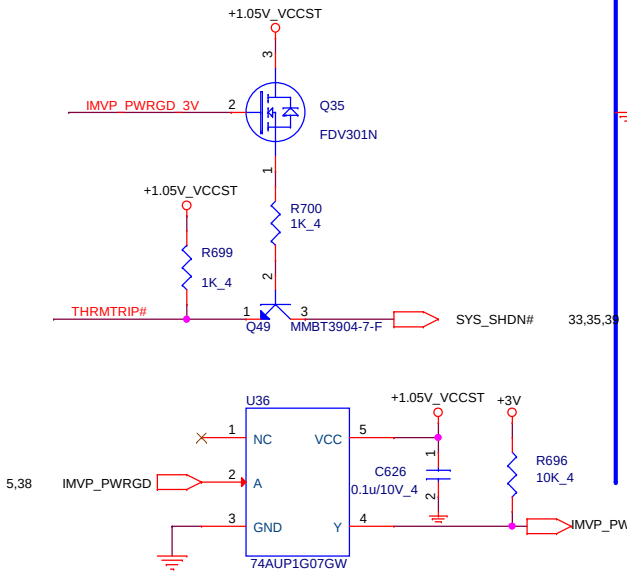
	Low	High
BOARD_ID0	N15V-GL-B	N15V-GM-B (Default)
BOARD_ID1	Reserved (Default)	Reserved
BOARD_ID2	Reserve for Touch pad, default(low)	
BOARD_ID3	WO/dTPM (Default)	W/dTPM
BOARD_ID4	w/VGA (Default)	wo/VGA

SKU ID



	SKU_ID1	SKU_ID0	VGA H/W Signal	Setup Menu	
UMA Only	0	0	UMA	Hidden	UMA boot
dGPU Only	0	1	GPU	Hidden	GPU boot
Switchable (Mux)	1	0	UMA+GPU	dGPU/SG	UMA boot
Optimize (Muxless)	1	1	UMA	UMA/SG	UMA boot

CPU thermal trip



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	LPT 4/6 (GPIO/MISC)	3A

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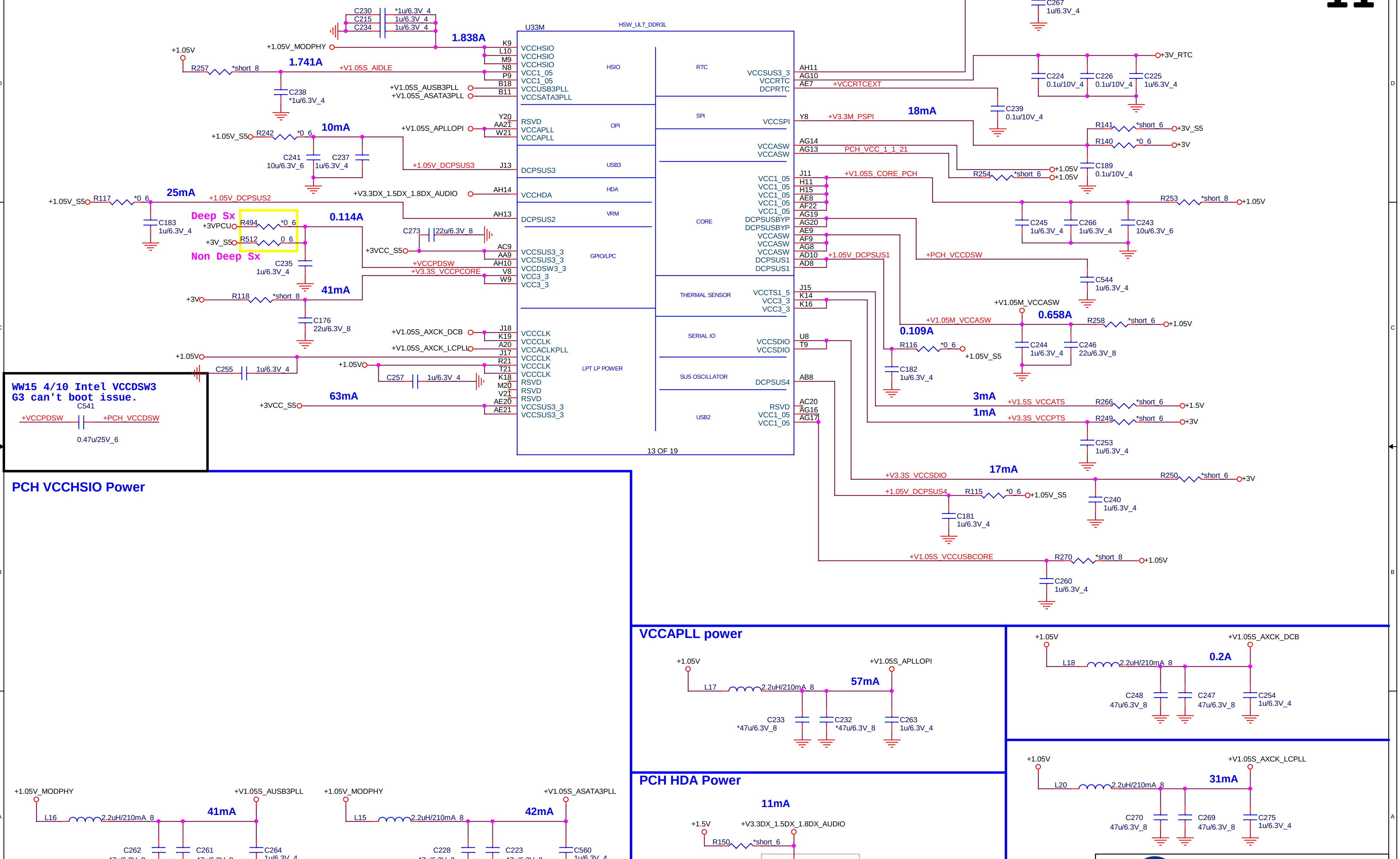
Haswell ULT PCH (Power)

11



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	LPT 5/6 (POWER)	3A
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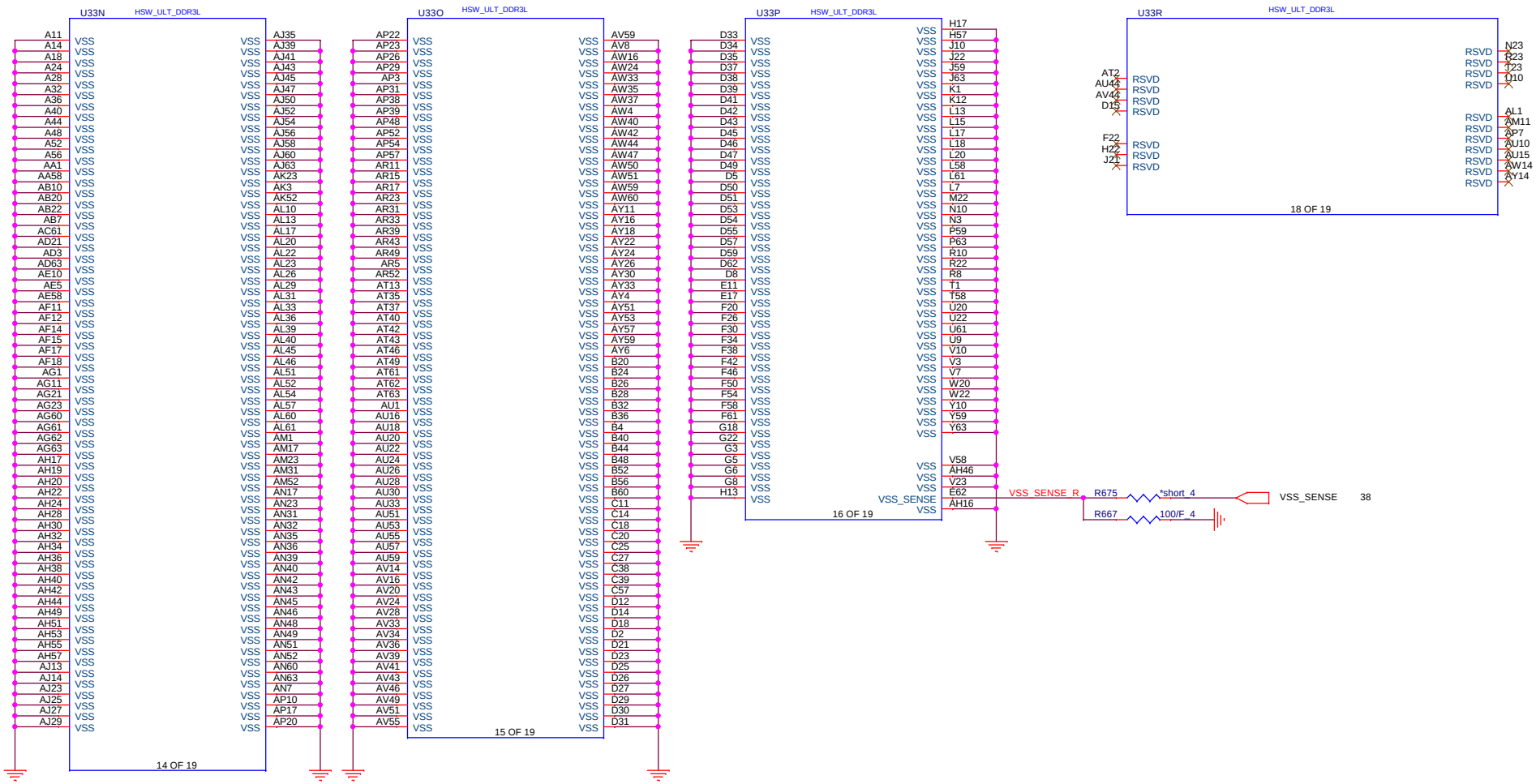
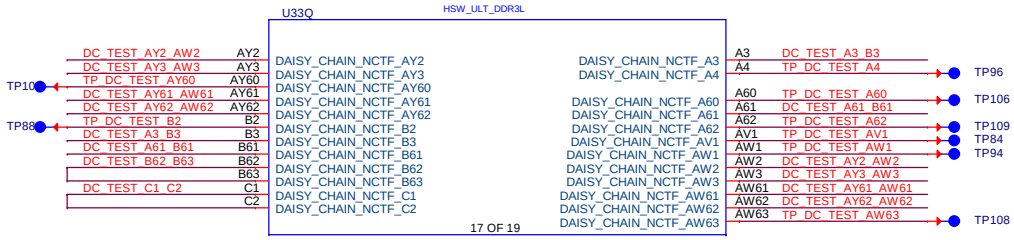
Haswell ULT (GND)





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	LPT 6/6 (GND)	3A

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Size	Document Number	Rev
	CPU/PCH XDP	3A

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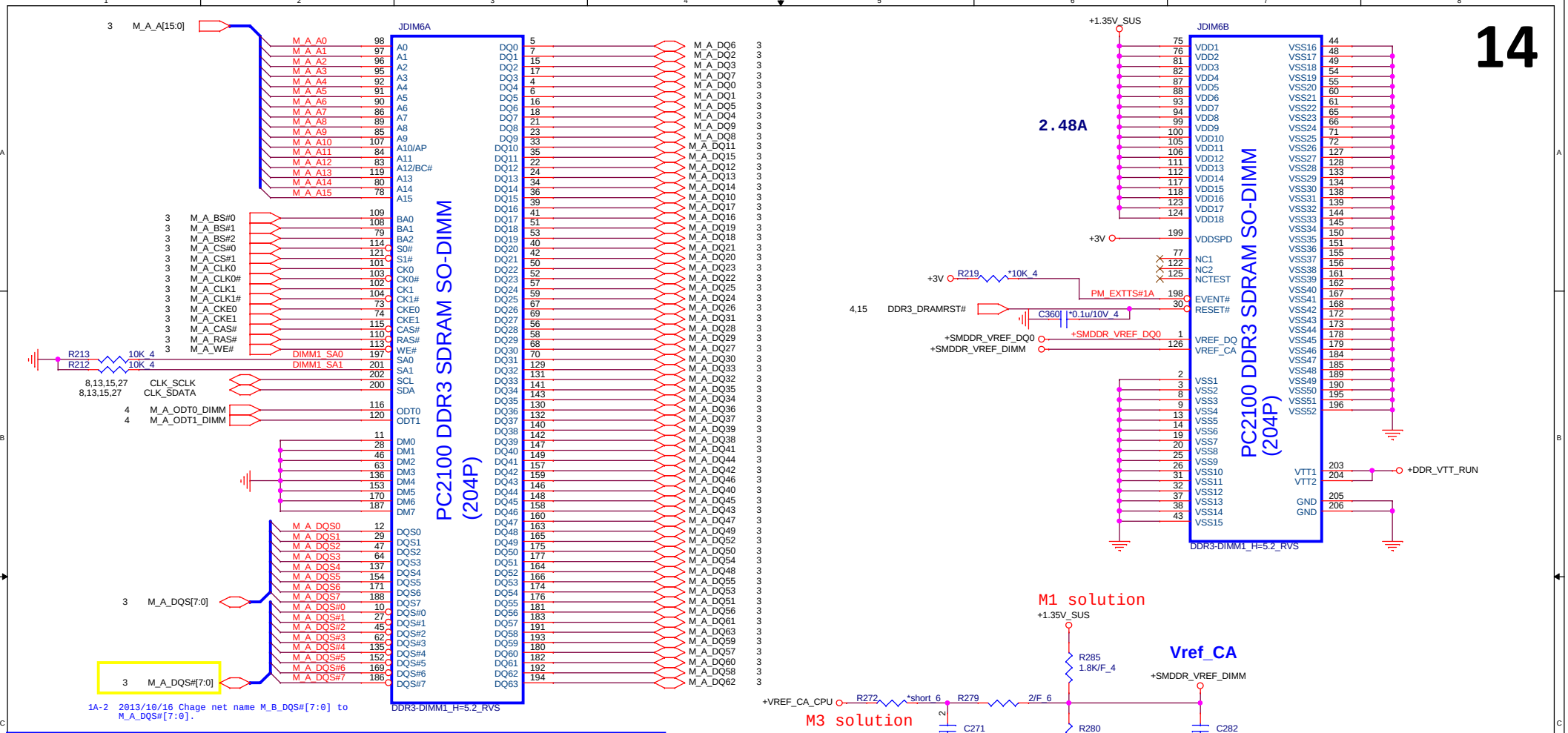

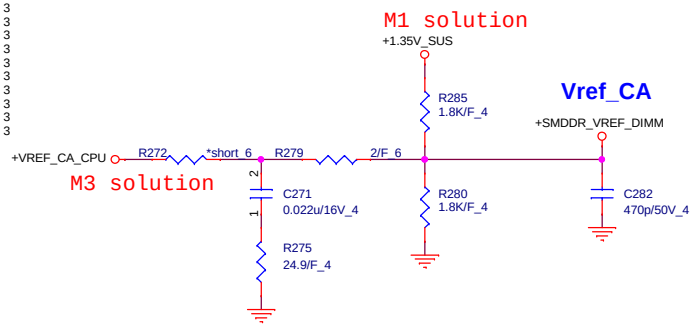

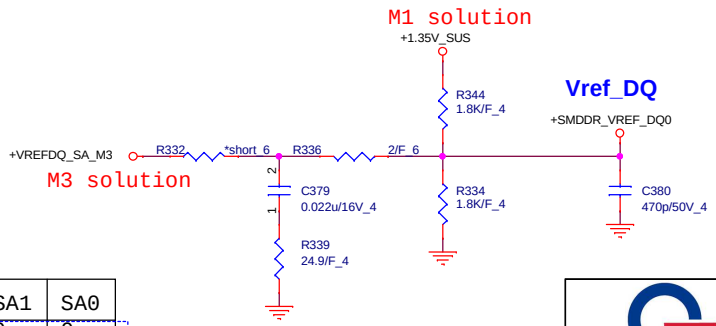

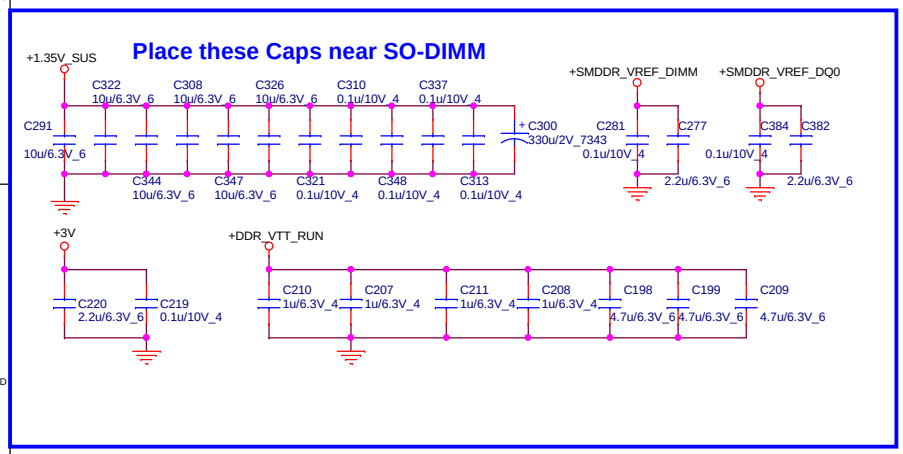

	SA1	SA0
CHA	0	0
CHB	1	0

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	DDR3 MEMORY SO-DIMM A	3A

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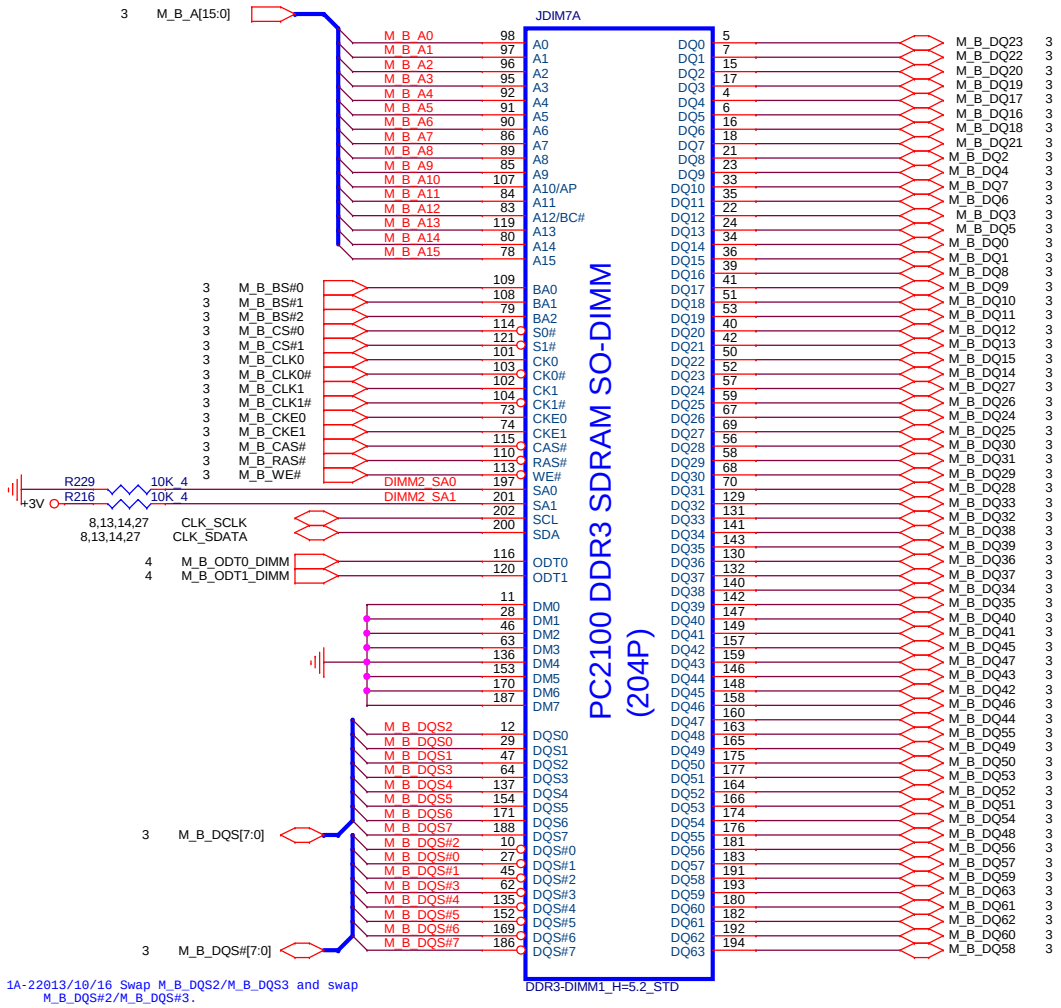
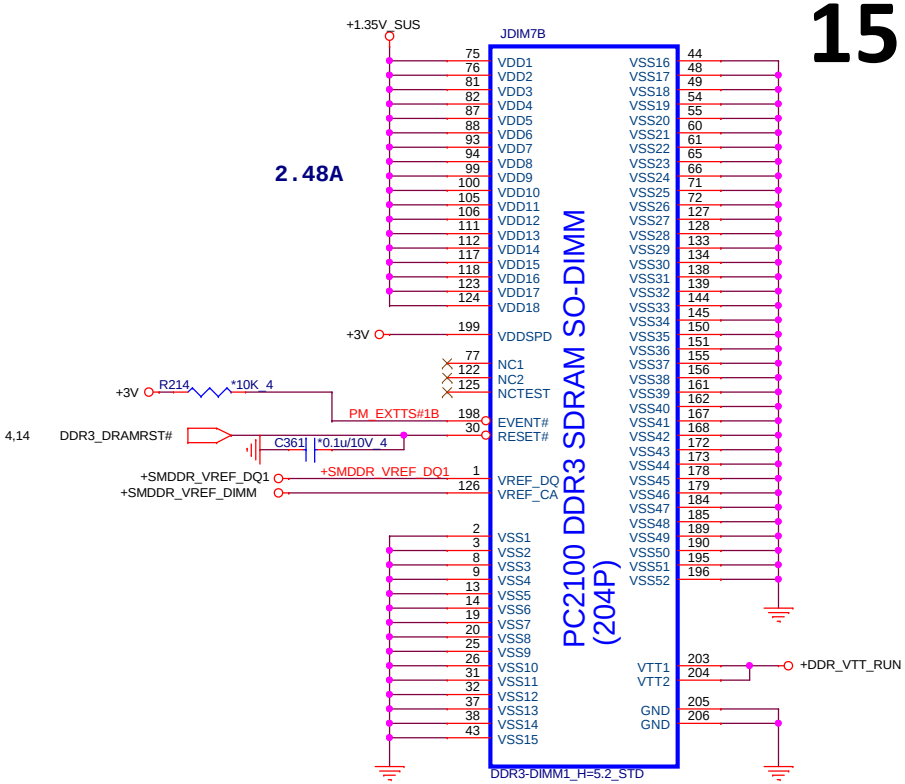
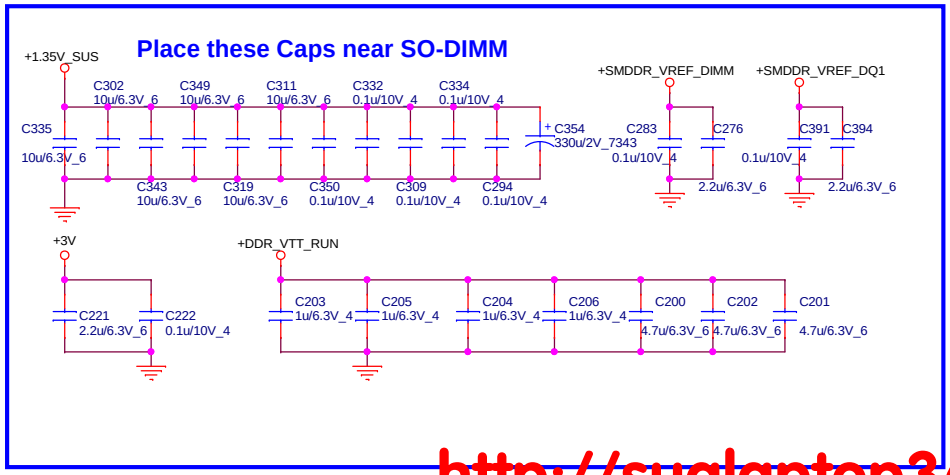
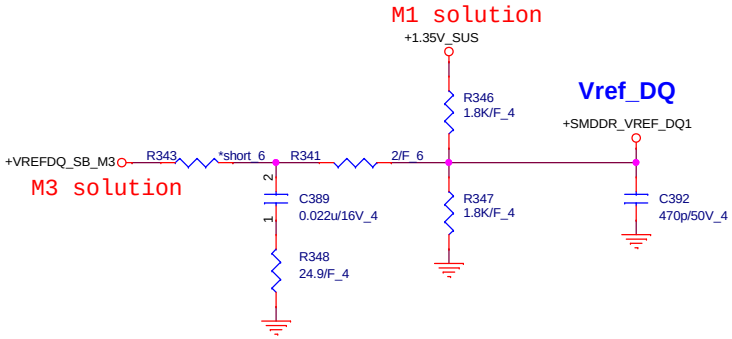


1A-22013/10/16 Swap M_B_DQS2/M_B_DQS3 and swap M_B_DQS#2/M_B_DQS#3.







	SA1	SA0
CHA	0	0
CHB	1	0

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Size	Document Number	Rev
	DDRIII Memory SO-DIMM B	3A

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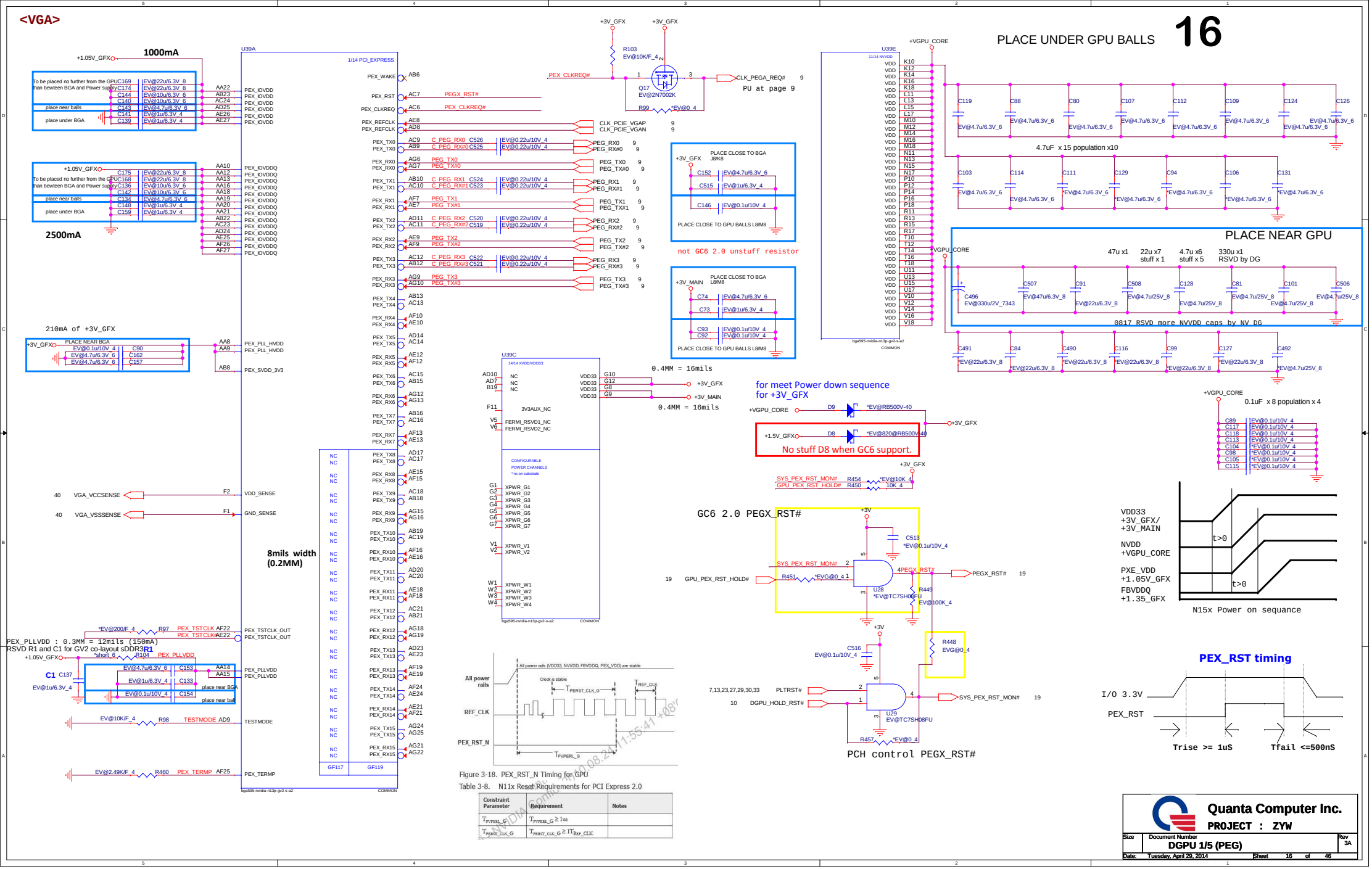

Figure 3-18. PEX_RST_N Timing for GPU

Table 3-8. N11x Reset Requirements for PCI Express 2.0

Constraint Parameter	Requirement	Notes
T_{PVPERL_G}	$T_{PVPERL\_G} \geq 1us$	
$T_{PERST\_CLK\_G}$	$T_{PERST\_CLK\_G} \geq 1T_{REF\_CLK}$	

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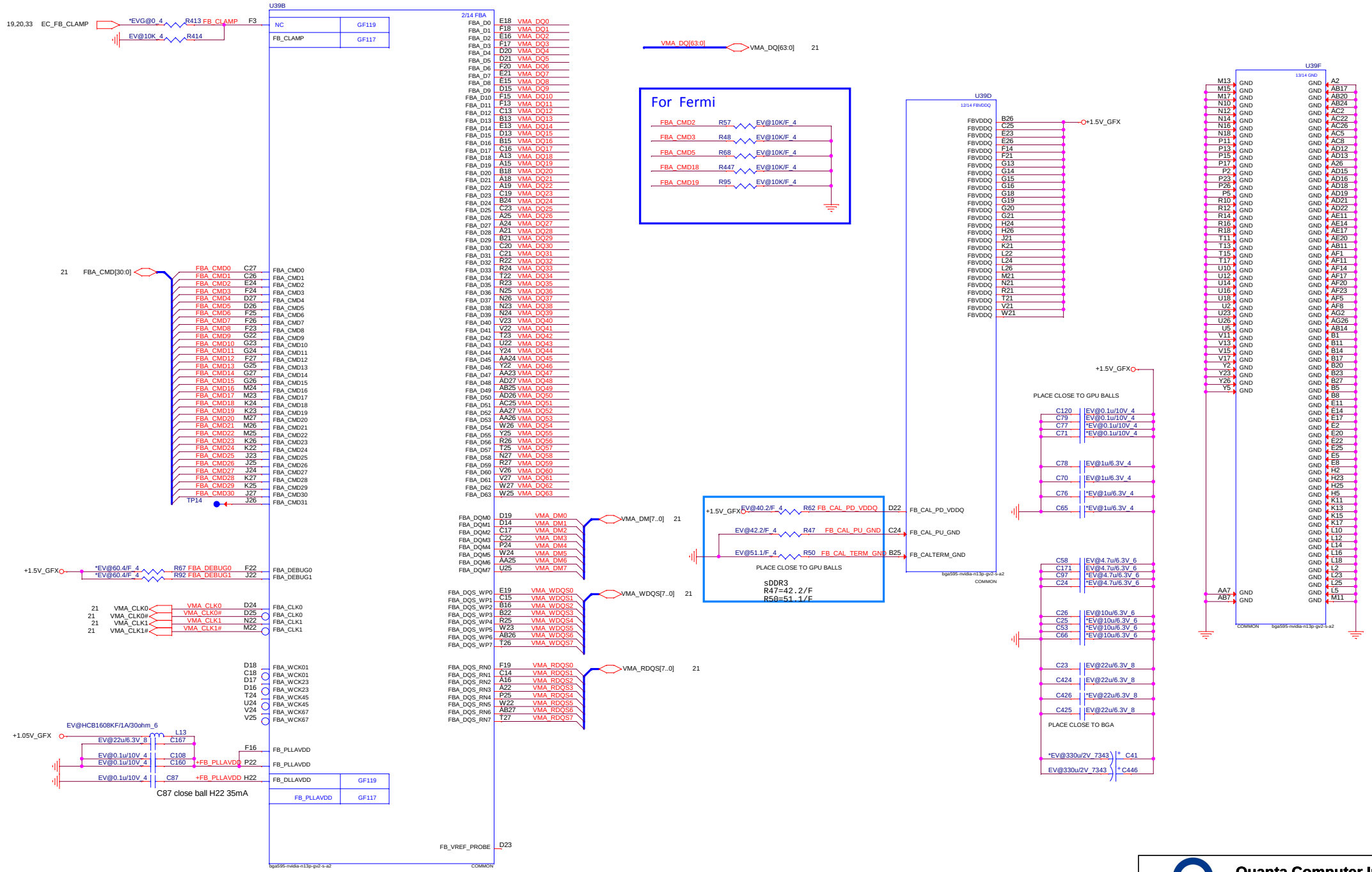
<VGA>



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Size	Document Number	Rev
	DGPU 2/5 (Memory)	3A

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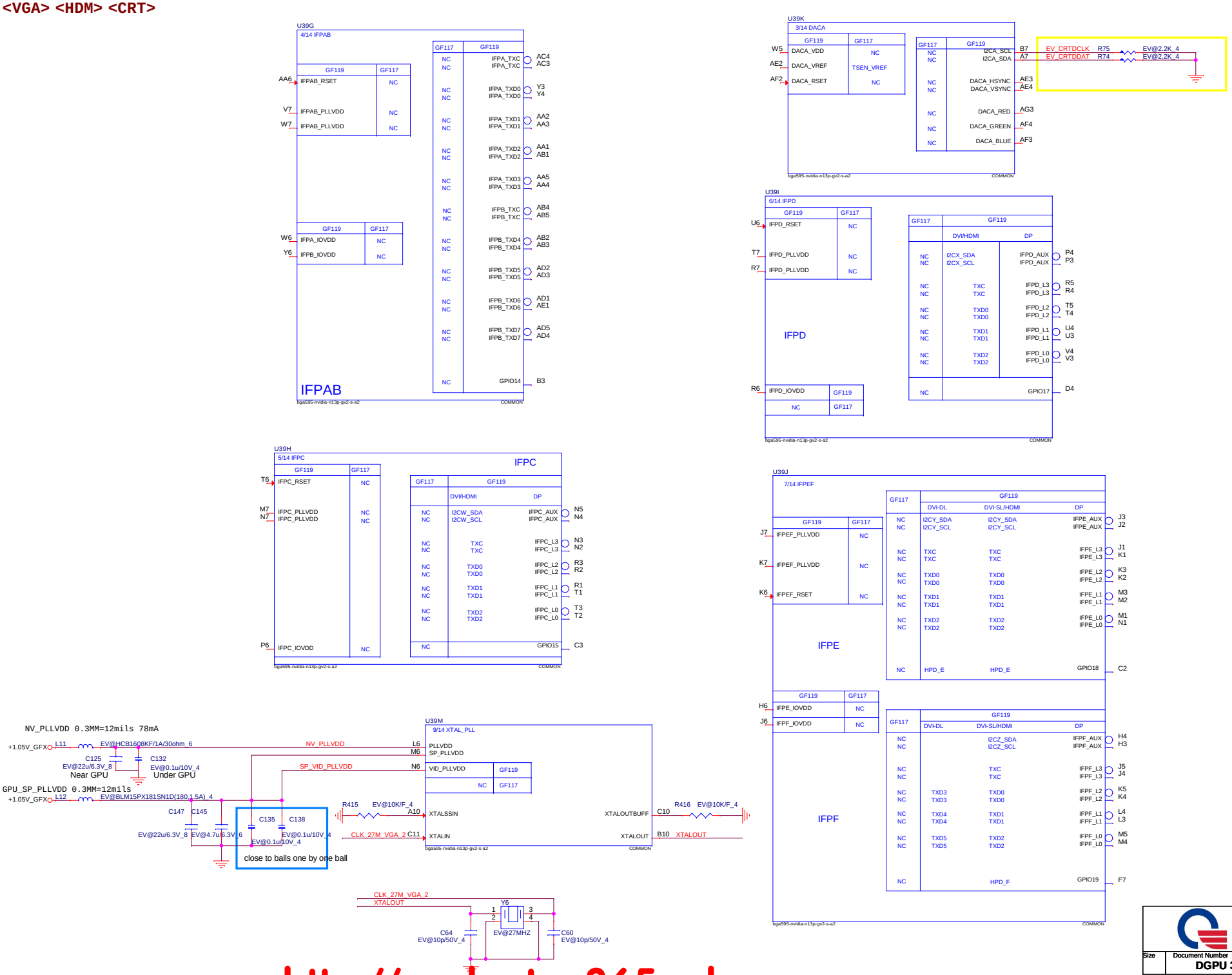
<VGA> <HDM> <CRT>



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Size	Document Number	Rev
	DGPU 3/5 (Display)	3A

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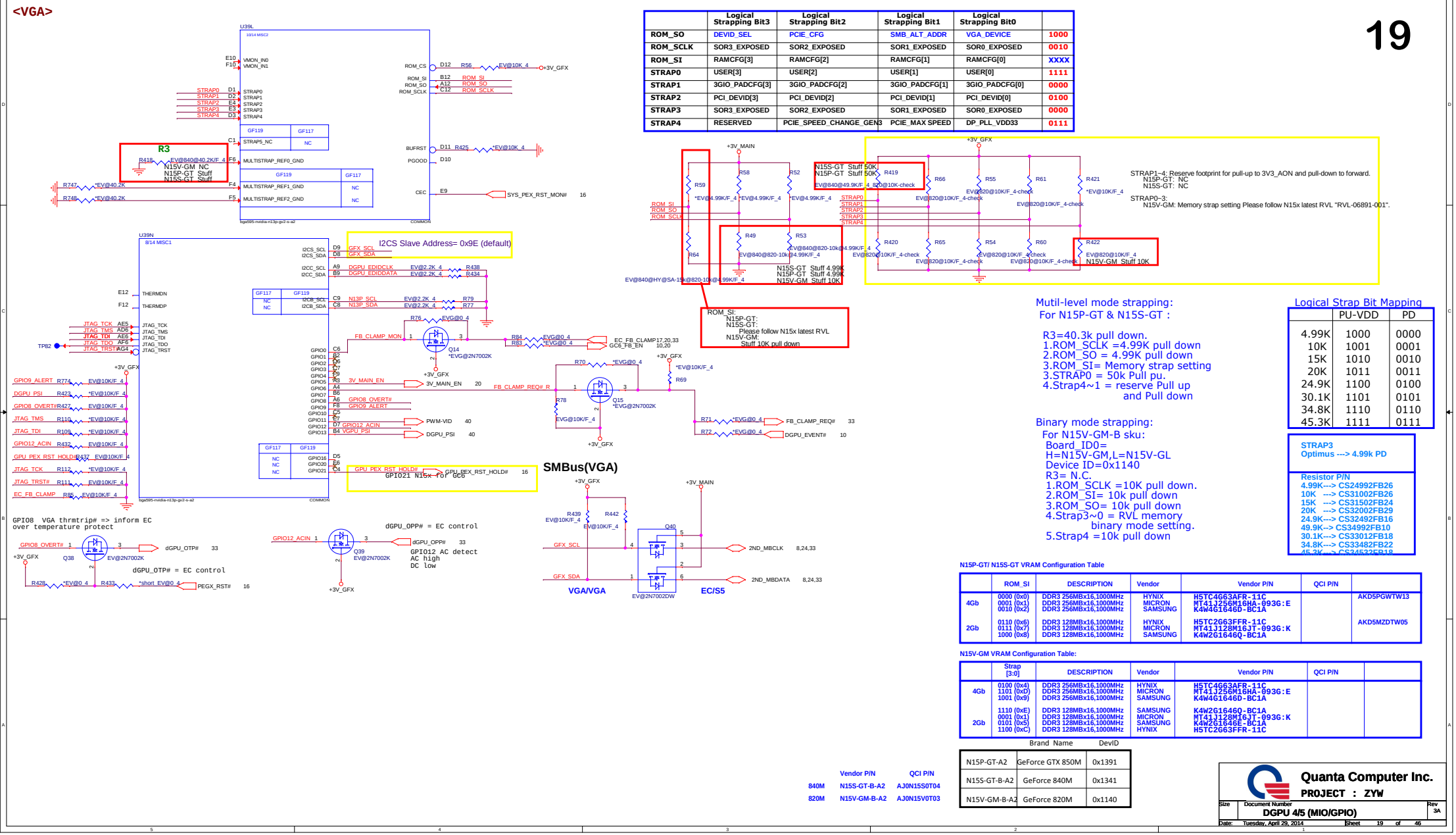

	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0	
ROM_SO	DEVID_SEL	PCIE_CFG	SMB_ALT_ADDR	VGA_DEVICE	1000
ROM_SCLK	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED	0010
ROM_SI	RAMCFG[3]	RAMCFG[2]	RAMCFG[1]	RAMCFG[0]	XXXX
STRAP0	USER[3]	USER[2]	USER[1]	USER[0]	1111
STRAP1	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]	0000
STRAP2	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]	0100
STRAP3	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED	0000
STRAP4	RESERVED	PCIE_SPEED_CHANGE_GEN3	PCIE_MAX SPEED	DP_PLL_VDD33	0111

Mutil-level mode strapping:
For N15P-GT & N15S-GT :

R3=40.3k pull down.
1.ROM_SCLK =4.99K pull down
2.ROM_SO = 4.99K pull down
3.ROM_SI= Memory strap setting
3.STRAP0 = 50k Pull pu.
4.Strap4~1 = reserve Pull up
and Pull down

Binary mode strapping:
For N15V-GM-B sku:
Board_ID0=
H=N15V-GM,L=N15V-GL
Device ID=0x1140
R3= N.C.
1.ROM_SCLK =10K pull down.
2.ROM_SI= 10k pull down
3.ROM_SO= 10k pull down
4.Strap3~0 = RVL memory
binary mode setting.
5.Strap4 =10k pull down

Logical Strap Bit Mapping

	PU-VDD	PD
4.99K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
24.9K	1100	0100
30.1K	1101	0101
34.8K	1110	0110
45.3K	1111	0111

STRAP3
Optimus ---> 4.99k PD

Resistor P/N
4.99K---> CS24992FB26
10K ---> CS31002FB26
15K ---> CS31502FB24
20K ---> CS32002FB29
24.9K---> CS32492FB16
49.9K--> CS34992FB10
30.1K---> CS33012FB18
34.8K---> CS33482FB22
45.3K---> CS34532FB18

N15P-GT/ N15S-GT VRAM Configuration Table

	ROM_SI	DESCRIPTION	Vendor	Vendor P/N	QCI P/N	
4Gb	0000 (0x0)	DDR3 256MBx16,1000MHz	HYNIX	H5TC4G63AFR-11C		AKD5PGWTW13
	0001 (0x1)	DDR3 256MBx16,1000MHz	MICRON	MT41J256M16HA-093G:E		
	0010 (0x2)	DDR3 256MBx16,1000MHz	SAMSUNG	K4W4G1646D-BC1A		
2Gb	0110 (0x6)	DDR3 128MBx16,1000MHz	HYNIX	H5TC2G63FFR-11C		AKD5MZDTW05
	0111 (0x7)	DDR3 128MBx16,1000MHz	MICRON	MT41J128M16JT-093G:K		
	1000 (0x8)	DDR3 128MBx16,1000MHz	SAMSUNG	K4W2G1646Q-BC1A		

N15V-GM VRAM Configuration Table:

	Strap [3:0]	DESCRIPTION	Vendor	Vendor P/N	QCI P/N	
4Gb	0100 (0x4)	DDR3 256MBx16,1000MHz	HYNIX	H5TC4G63AFR-11C		
	1101 (0x3)	DDR3 256MBx16,1000MHz	MICRON	MT41J256M16HA-093G:E		
	1001 (0x9)	DDR3 256MBx16,1000MHz	SAMSUNG	K4W4G1646D-BC1A		
2Gb	1110 (0xE)	DDR3 128MBx16,1000MHz	SAMSUNG	K4W2G1646Q-BC1A		
	0001 (0x1)	DDR3 128MBx16,1000MHz	MICRON	MT41J128M16JT-093G:K		
	0101 (0x5)	DDR3 128MBx16,1000MHz	SAMSUNG	K4W2G1646E-BC1A		
	1100 (0xC)	DDR3 128MBx16,1000MHz	HYNIX	H5TC2G63FFR-11C		

	Brand Name	DevID
N15P-GT-A2	GeForce GTX 850M	0x1391
N15S-GT-B-A2	GeForce 840M	0x1341
N15V-GM-B-A2	GeForce 820M	0x1140

	Vendor P/N	QCI P/N
840M	N15S-GT-B-A2	AJ0N15S0T04
820M	N15V-GM-B-A2	AJ0N15V0T03

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	DGPU 4/5 (MIO/GPIO)	3A

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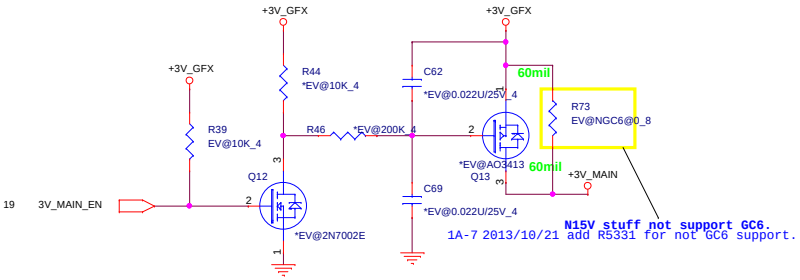
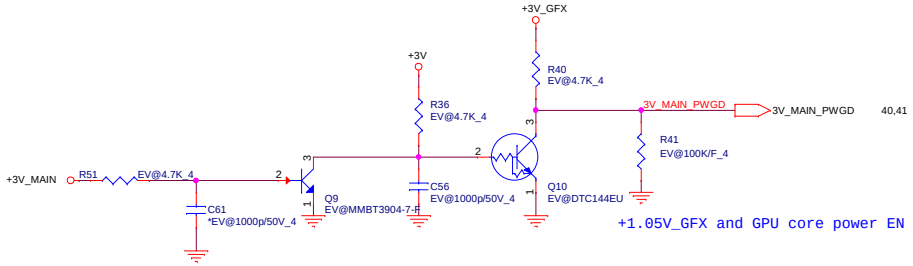
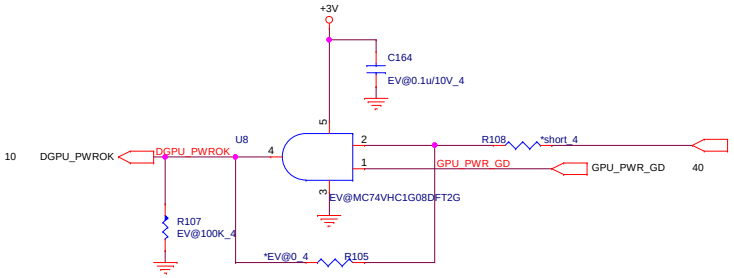
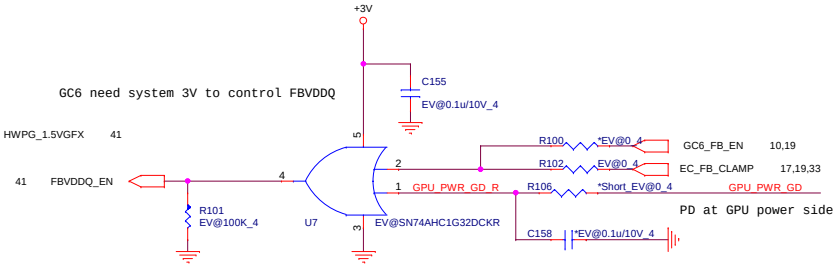
3V MAIN POWER







GC6 need system 3V to control FBVDDQ



PD at GPU power side

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Size	Document Number	Rev
	DGPU 5/5 (Power/Ground)	3A

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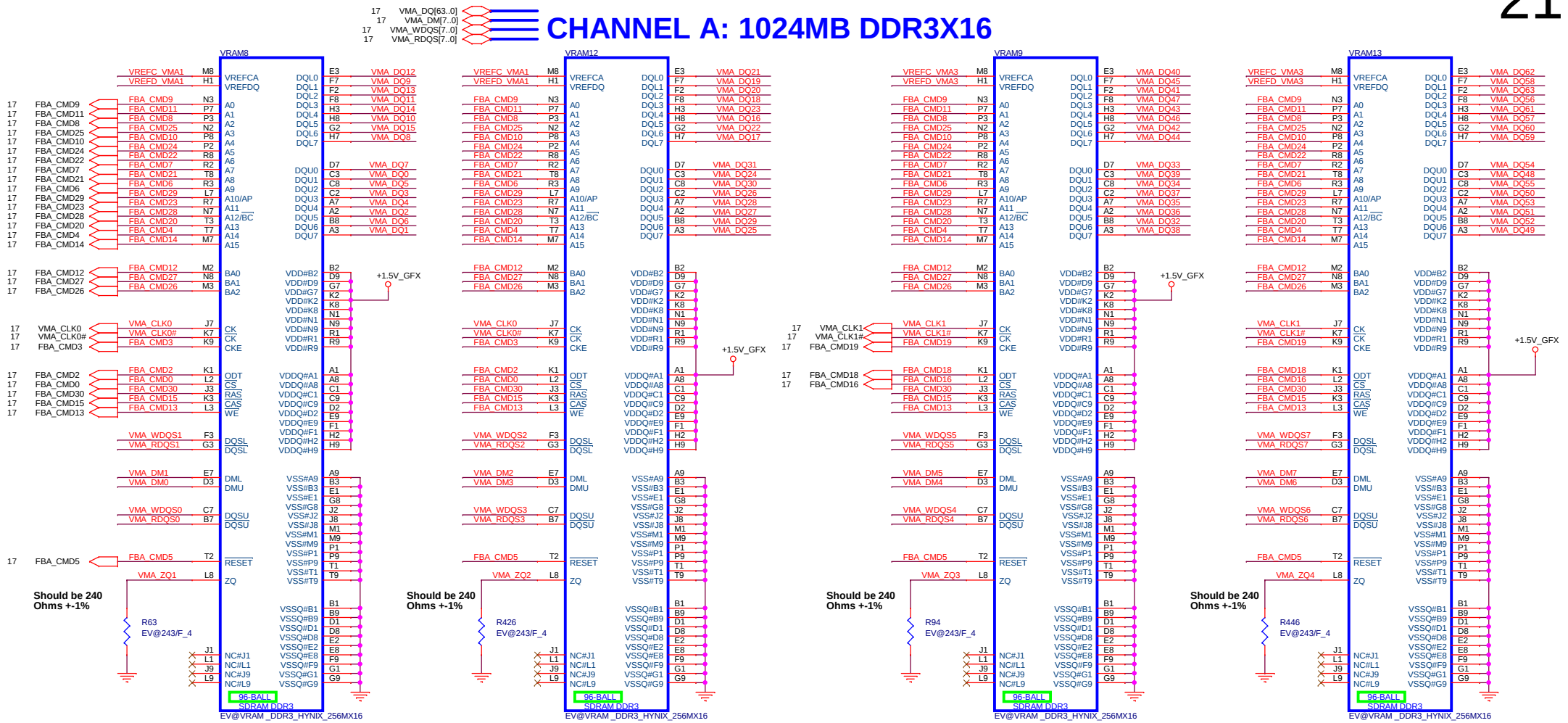
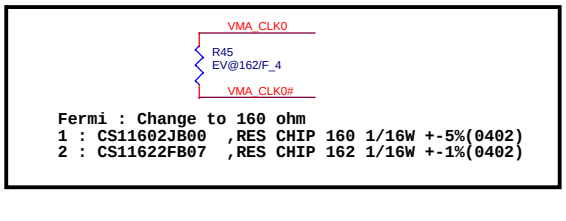
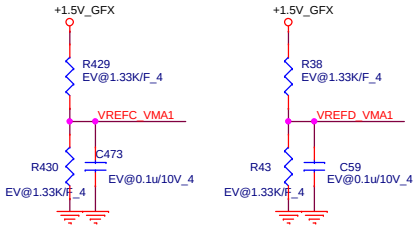
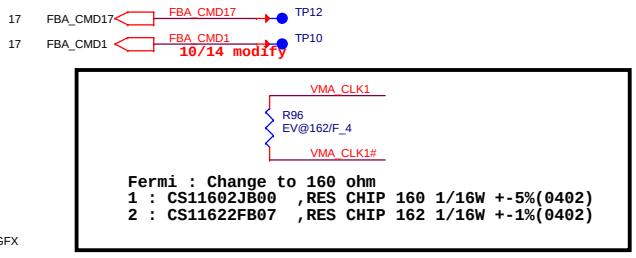
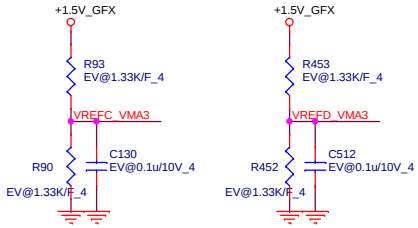
CHANNEL A: 1024MB DDR3X16

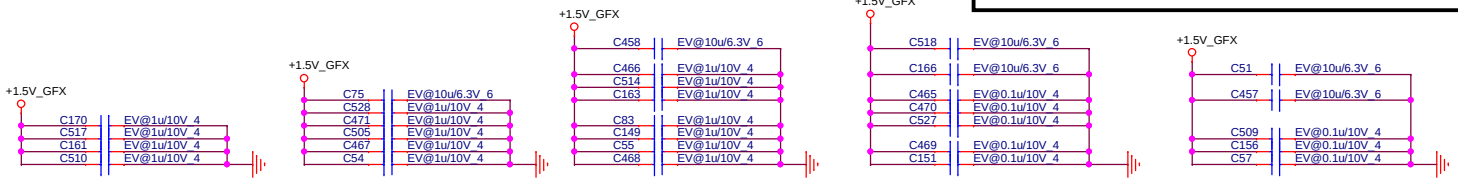












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Size	Document Number	Rev
	N15P- DDR3 VRAM 1/2	3A

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Size	Document Number	Rev
	N13P DDR3 VRAM 2/2	3A

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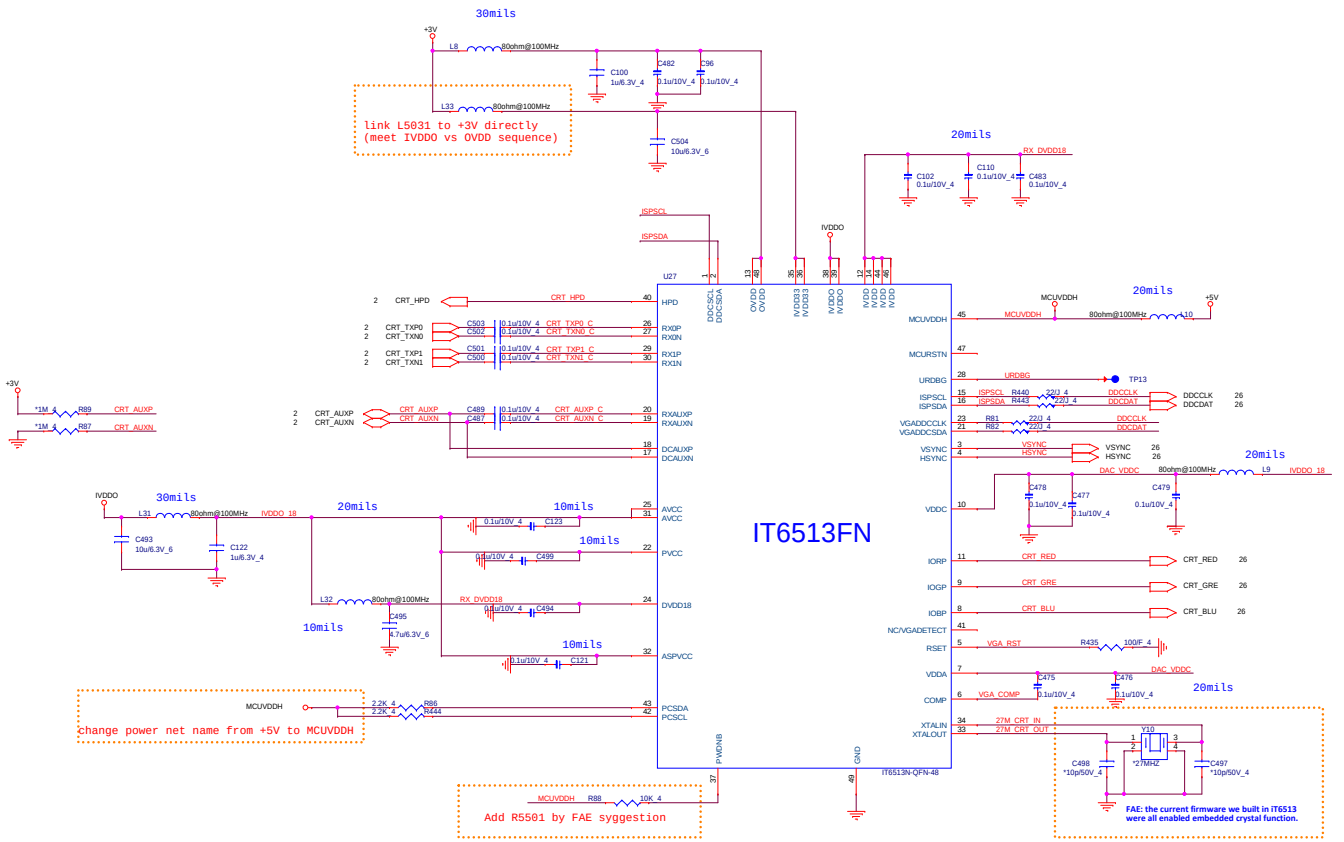
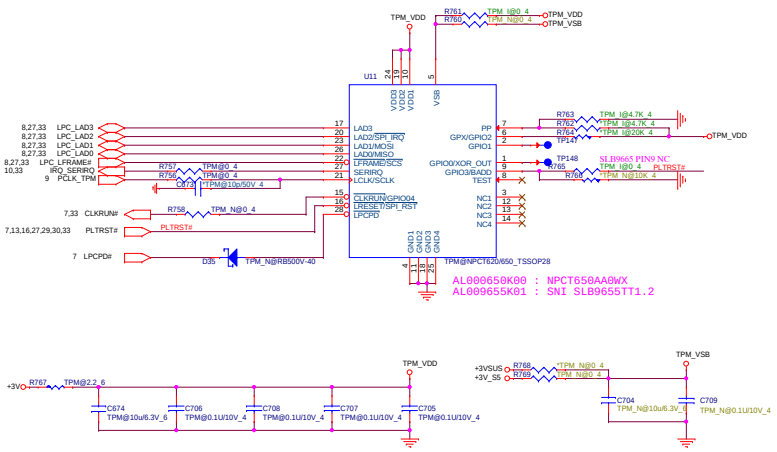
DP TO VGA



TPM (TPM)

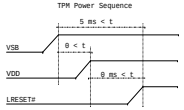


NPCT650AA0WX infromation:

NOTE:
1) The PP is an input signal with configurable polarity.
2) By default the PP functionality is disabled.

NOTE:
GPX signal is connected to the TCS_EN signal
of the PCI Express Root Complex of chipset.

NOTE:
GPIO_IF[0..3], GPX and PP are optional.
Leave them open if not used.



NOTE:
1) It is recommended to connect the TPM to the system's standby voltage to improve performance.
2) If only one power plane is available in the system, connect both VSB and VDD to that power source.
3) LRESET# must be asserted for at least 5 msec after VSB power-up.
4) VSB may come up anytime before VDD power-up, but not after VDD power-up.

GPIO_IF3

BADD	SELECTION
0	EEh - EFh
1	7Eh - 7Fh

'1' - pin is left open.
'0' - pin is pulled down.

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Size	Document Number	Rev
	Mini DP/HD3SS2521	3A

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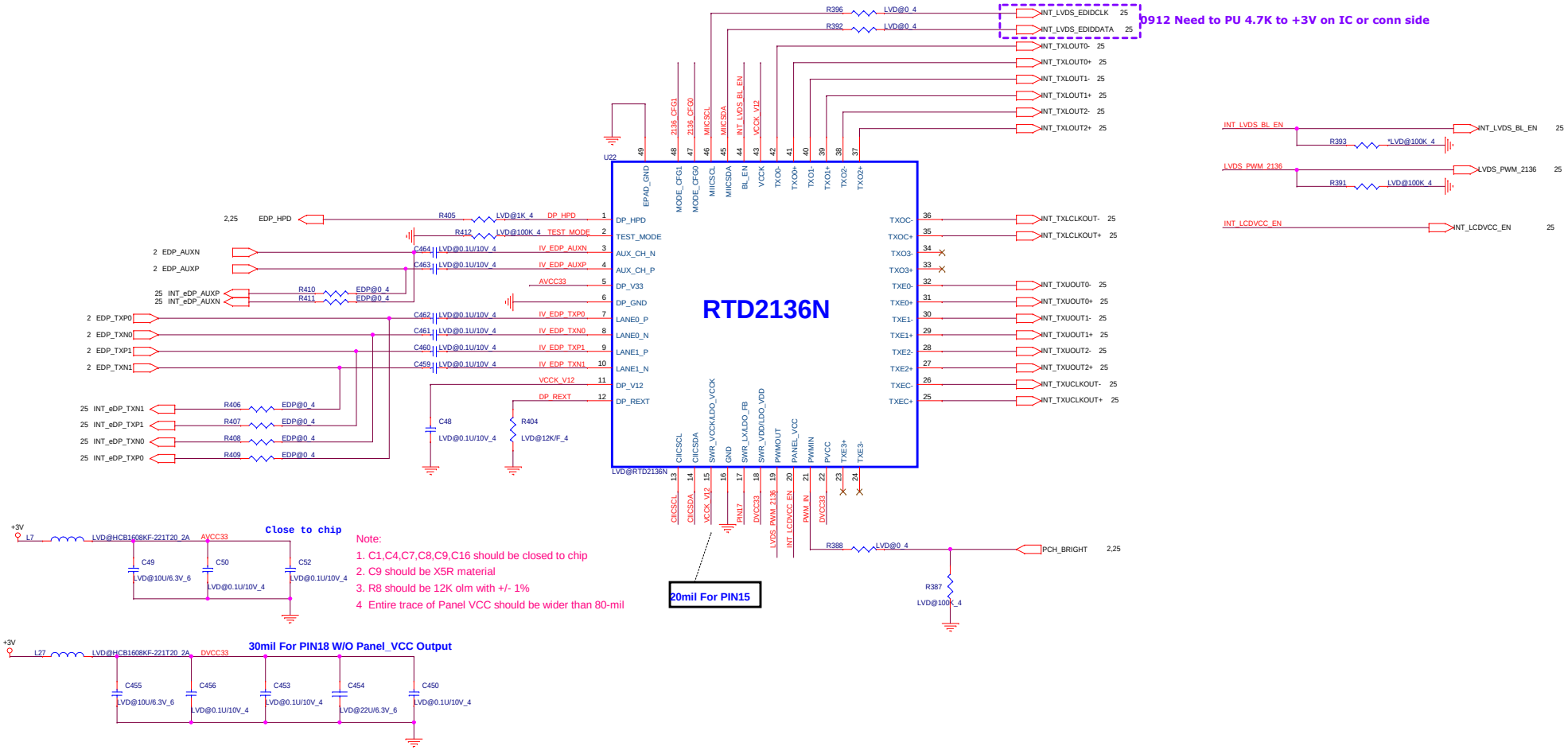
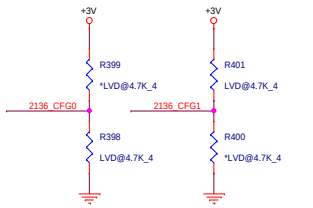


Mode Configure Table(Power On Latch)

		CFG0	
		0	1
CFG1	0	X	EP MODE
	1	ROM ONLY MODE	EEPROM MODE

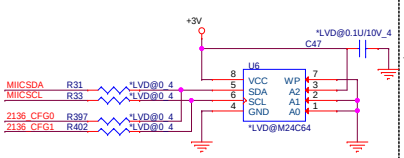
ROM ONLY Mode : CFG0 4.7K pull low, CFG1 4.7K pull high
EP Mode : CFG0 4.7K pull high, CFG1 4.7K pull low
EEPROM Mode : CFG0 4.7K pull high, CFG1 4.7K pull high



EEPROM Mode

In EEPROM mode, an additional EEPROM is needed.
EEPROM should configure with following condition.

1- EEPROM with a size 8K-Byte
2- EEPROM device should be 2-byte addressing device
3- Slave address should configure as 0xA8

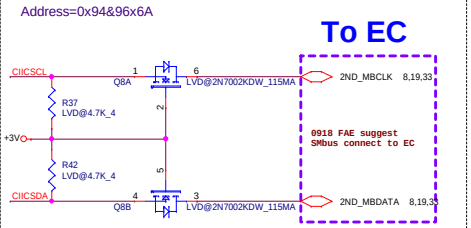


I2C address=0xA8

EP Mode

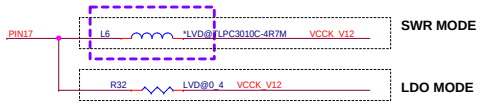
External device connect to DP2LVDS by
Pin13/Pin14, I2C protocol is used

Address=0x94&96x6A

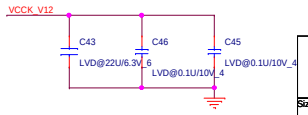


Dual Mode Regulator Configuration

	2.2-uH(L6)	0 Olm(R31)
SWR	Connect	NC
LDO	NC	Connect



1. C18 10-uF capacitor should be X5R material
2. Inductor should be withstand current >600-mA
3. Capacitors should be closed to PIN17



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Size	Document Number	Rev
	eDP to LVDS	3A

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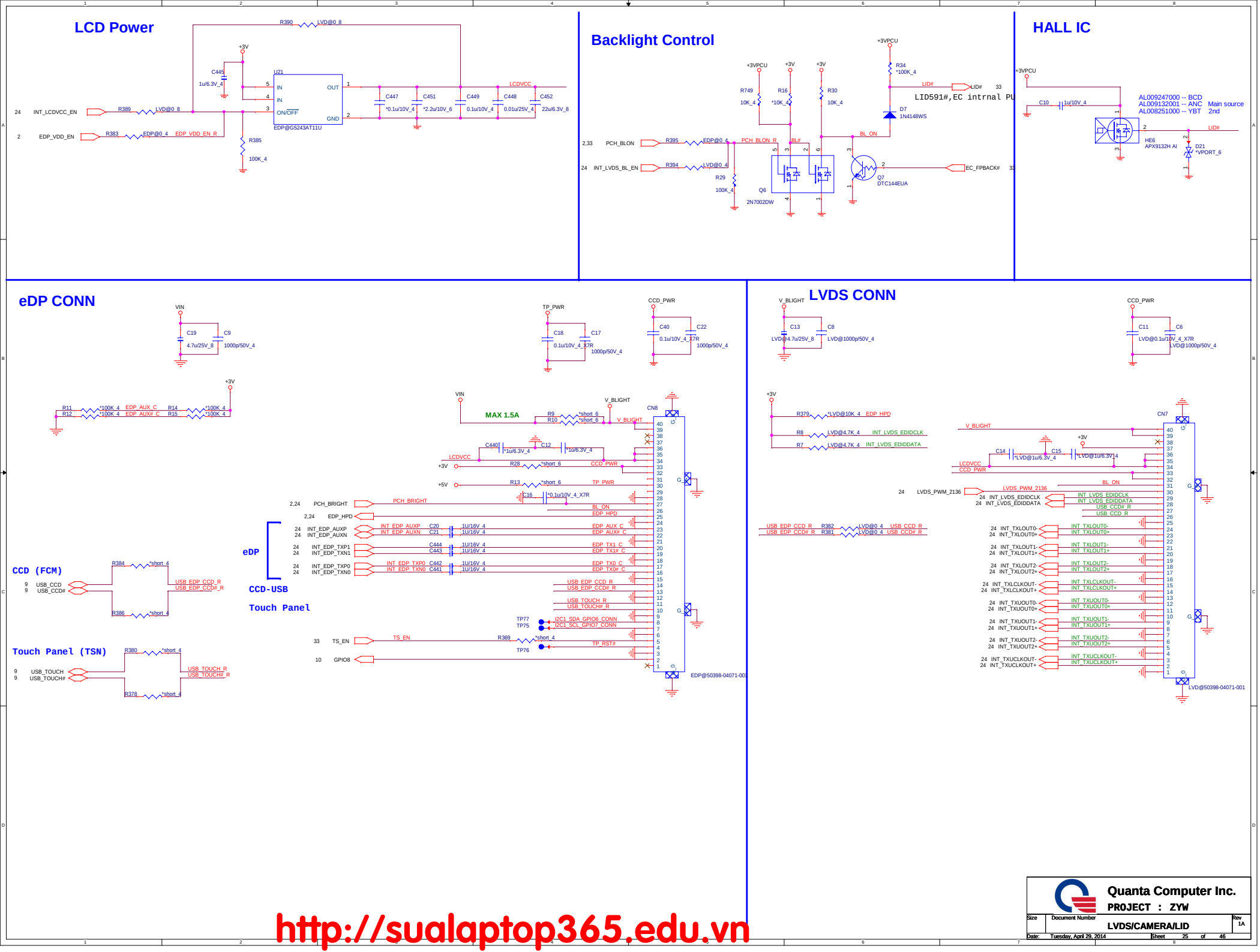

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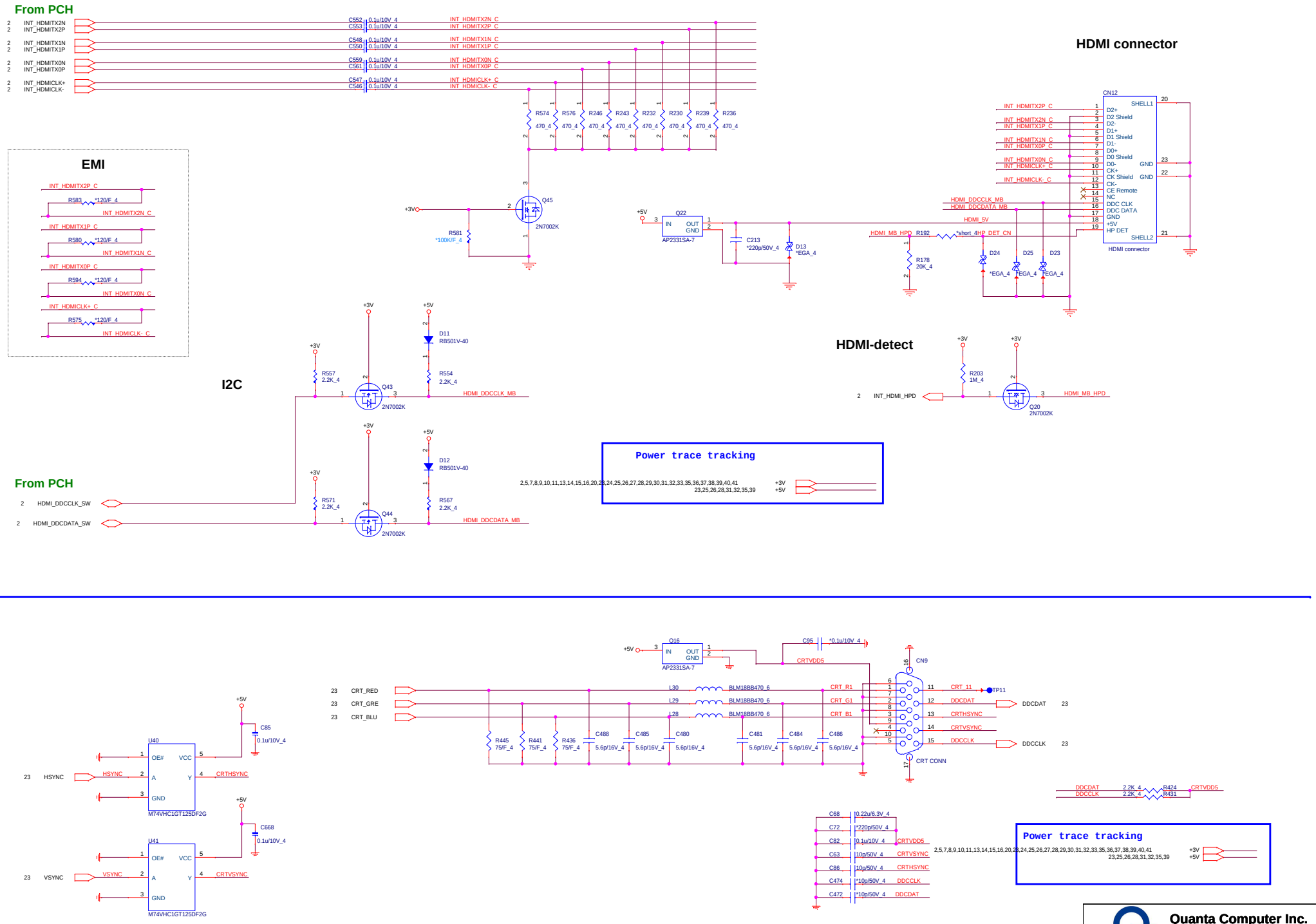
HDMI



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Size	Document Number	Rev
	HDMI (PS8101)	1A

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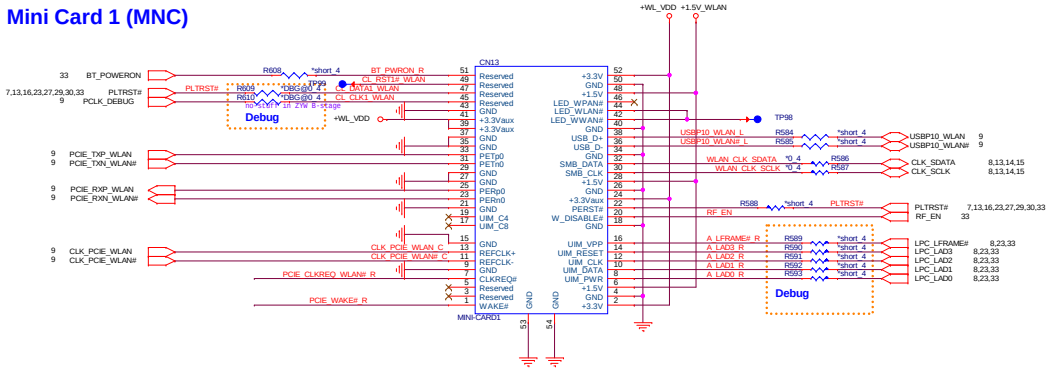
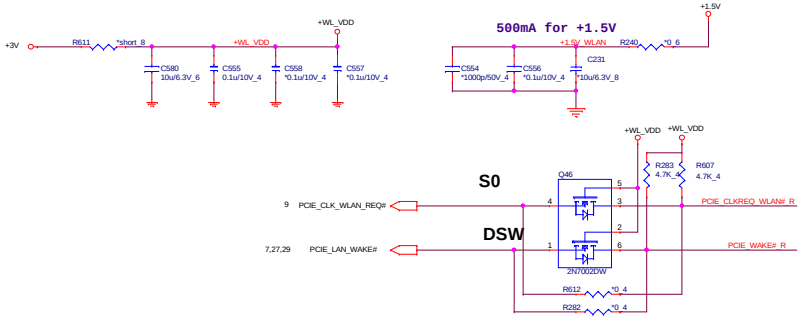
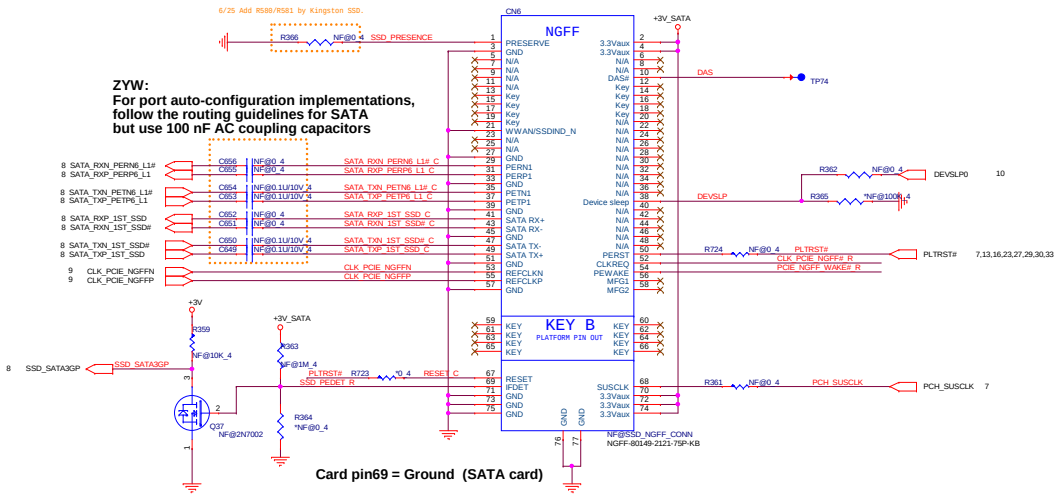
Mini Card 1 (MNC)

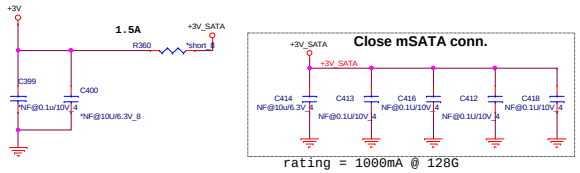


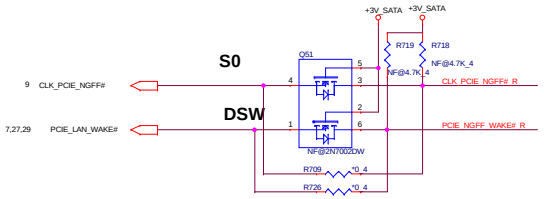


NGFF (NGF)



pin	Type	Description
1	PRESENCE	This pin is grounded on the SSD. May be used by host to determine if slot is empty or populated
10	DAS#	Device Activity Signal
21	WWAN/SSDIND_N	This pin connect to Ground
38	Device Sleep Signal	If system didn't support DEVSLP, set DEVSLP Sleep Signal pin power high and keep (from power on), device will ignore. If system support DEVSLP, set DEVSLP Sleep Signal pin power low (from power on) device, device will support DEVSLP function. Device Sleep Signal H: SSD enter sleep model. Device Sleep Signal L: SSD exit sleep model.
53	REFCLKN	no connect on SSD
55	REFCLKP	no connect on SSD
56	MFG1	Manufacturing pin. Use determined by vendor. Must be a noconnect on the host board
58	MFG2	Manufacturing pin. Use determined by vendor. Must be a noconnect on the host board
68	SUSCLK	no connect on SSD
69	IFDET	This pin connect to Ground





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Size	Document Number	Rev
	Mini-Card/NGFF	1A

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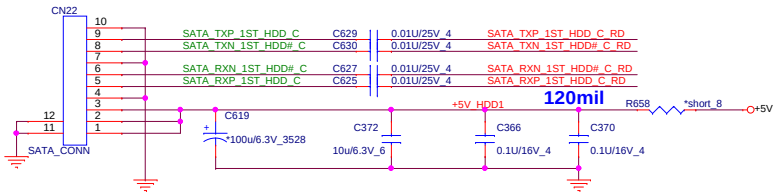
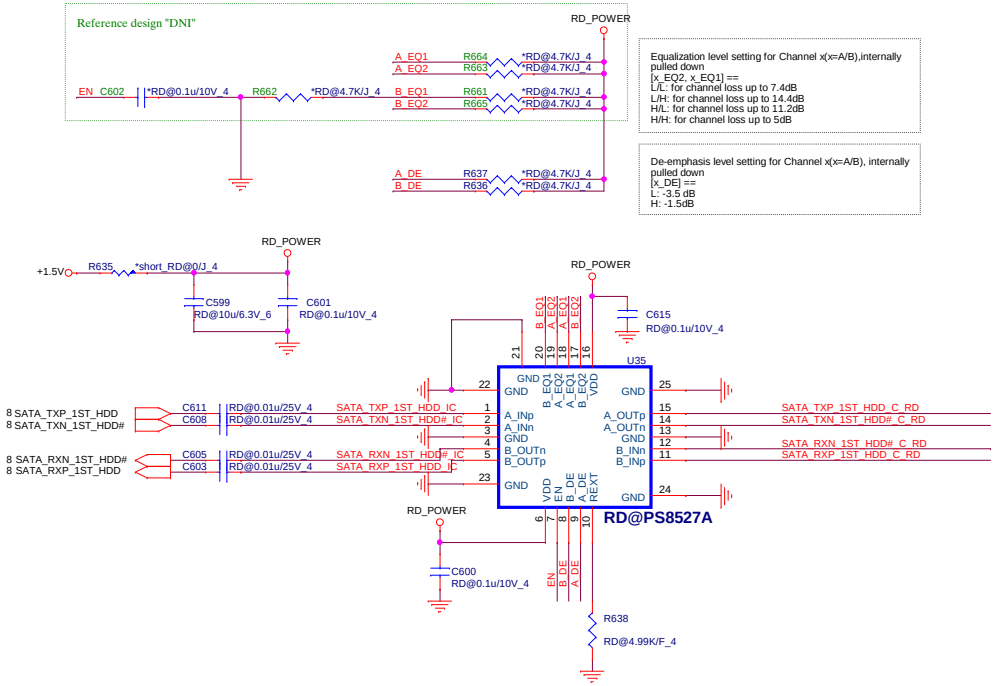
SATA HDD1

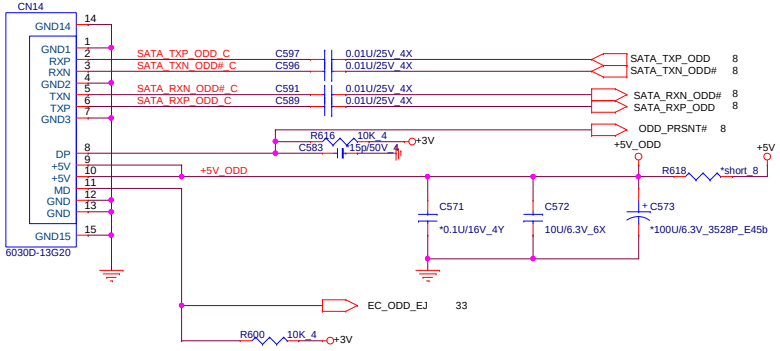
HDD1



HDD1 SATA Re-driver



ODD



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Quanta Computer Inc.
PROJECT : ZYW

Size	Document Number	Rev
	SATA HDD/LED/SW	1A

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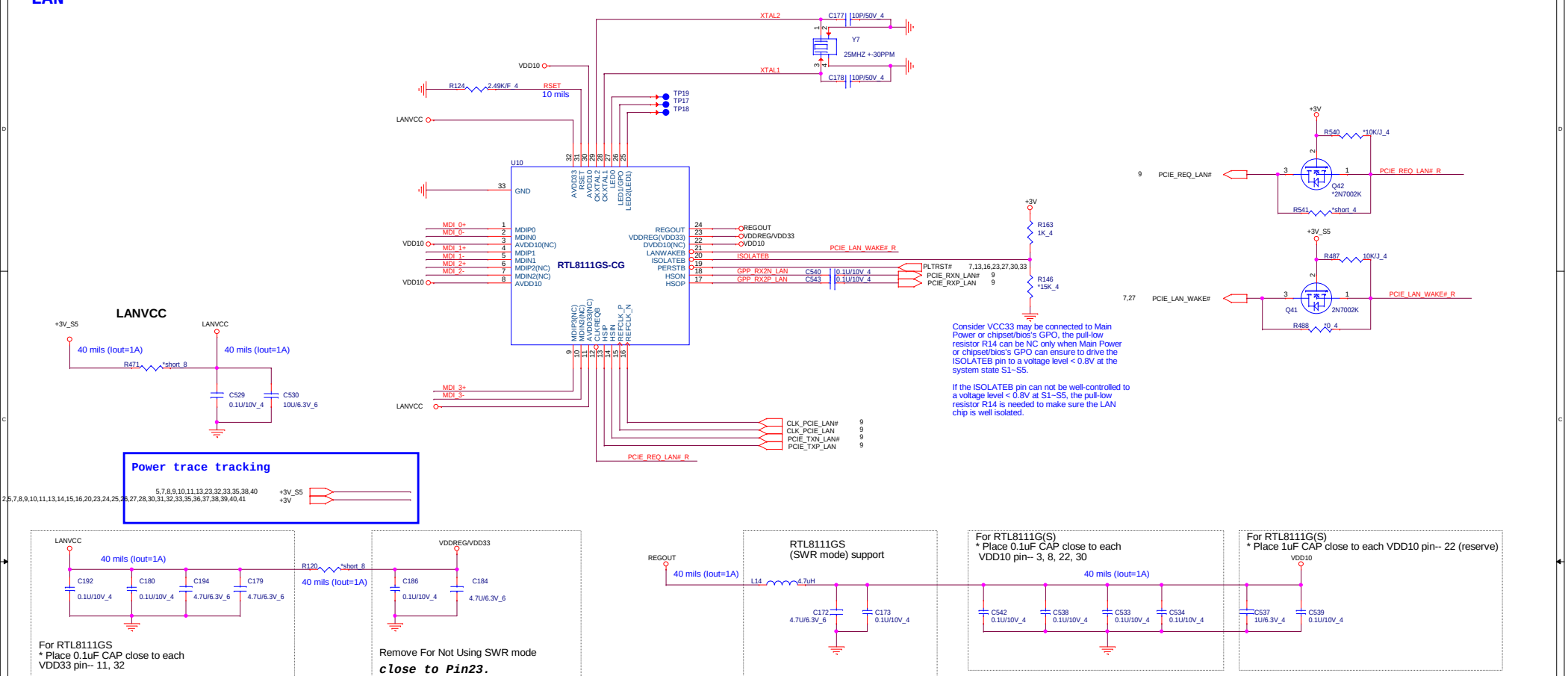
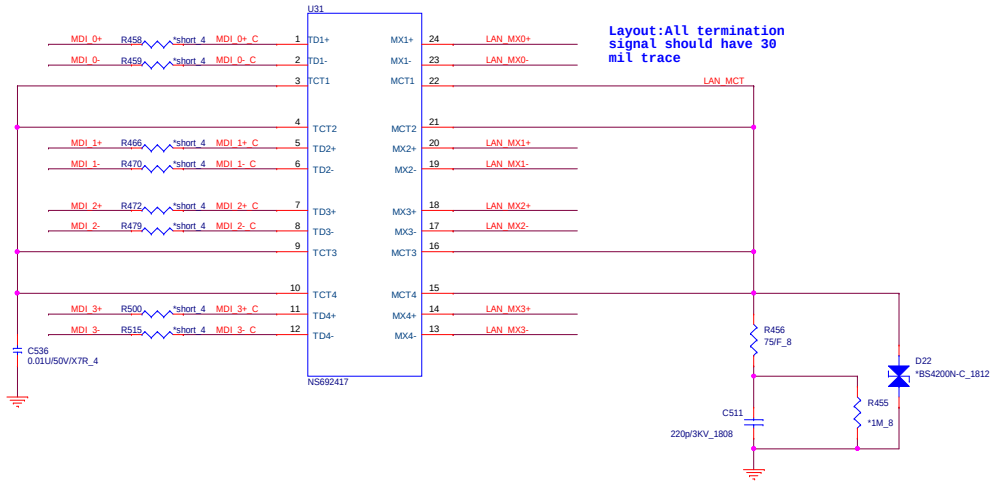
LAN



Consider VCC33 may be connected to Main Power or chipset/bios's GPO, the pull-low resistor R14 can be NC only when Main Power or chipset/bios's GPO can ensure to drive the ISOLATEB pin to a voltage level < 0.8V at the system state S1~S5.

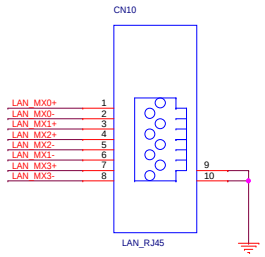
If the ISOLATEB pin can not be well-controlled to a voltage level < 0.8V at S1~S5, the pull-low resistor R14 is needed to make sure the LAN chip is well isolated.

Tramsformer



Layout:All termination signal should have 30 mil trace

RJ45 Connector



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PROJECT : ZYW		
Size	Document Number: LAN	Rev F3A
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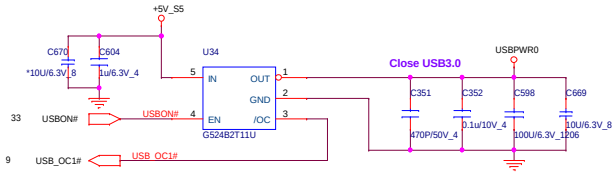
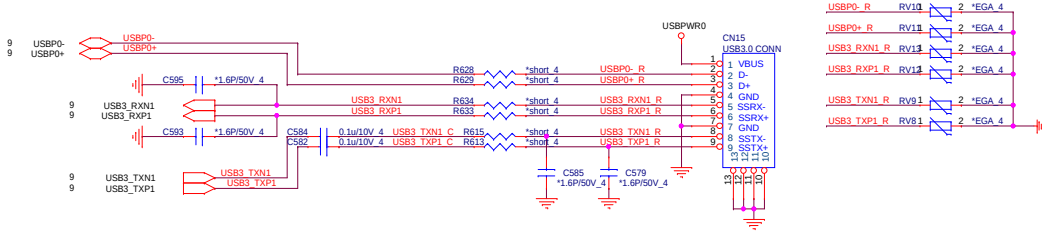
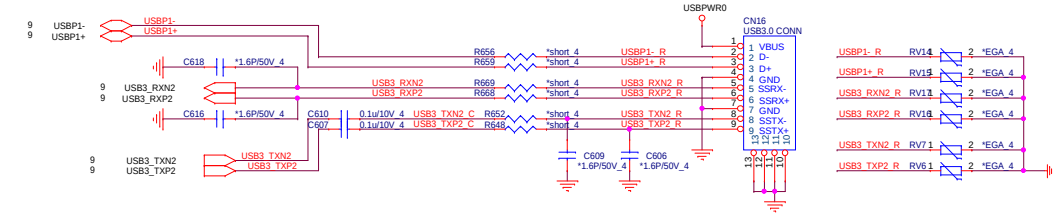
USB3.0 (UB3)

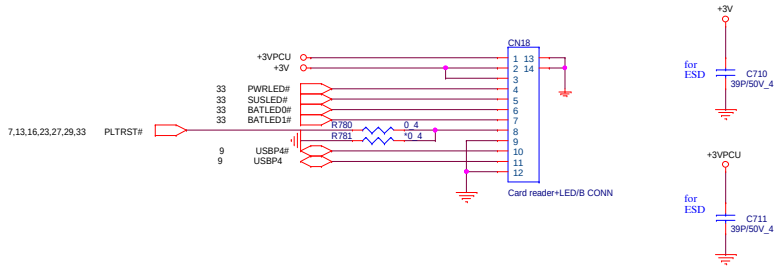


G524B2T11U: Enable: Low Active /2.5A

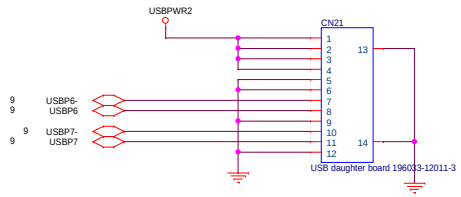


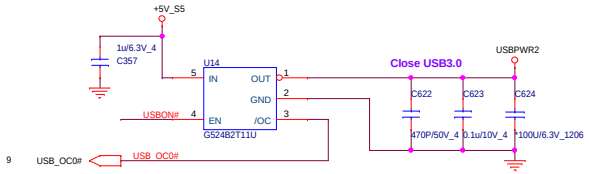


Card Reader+ LED/B Connector



USB D/B (UB2)





G524B2T11U: Enable: Low Active /2.5A

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Quanta Computer Inc.
PROJECT : ZYW

Size	Document Number	Rev
	USB3(S&C)	F3A

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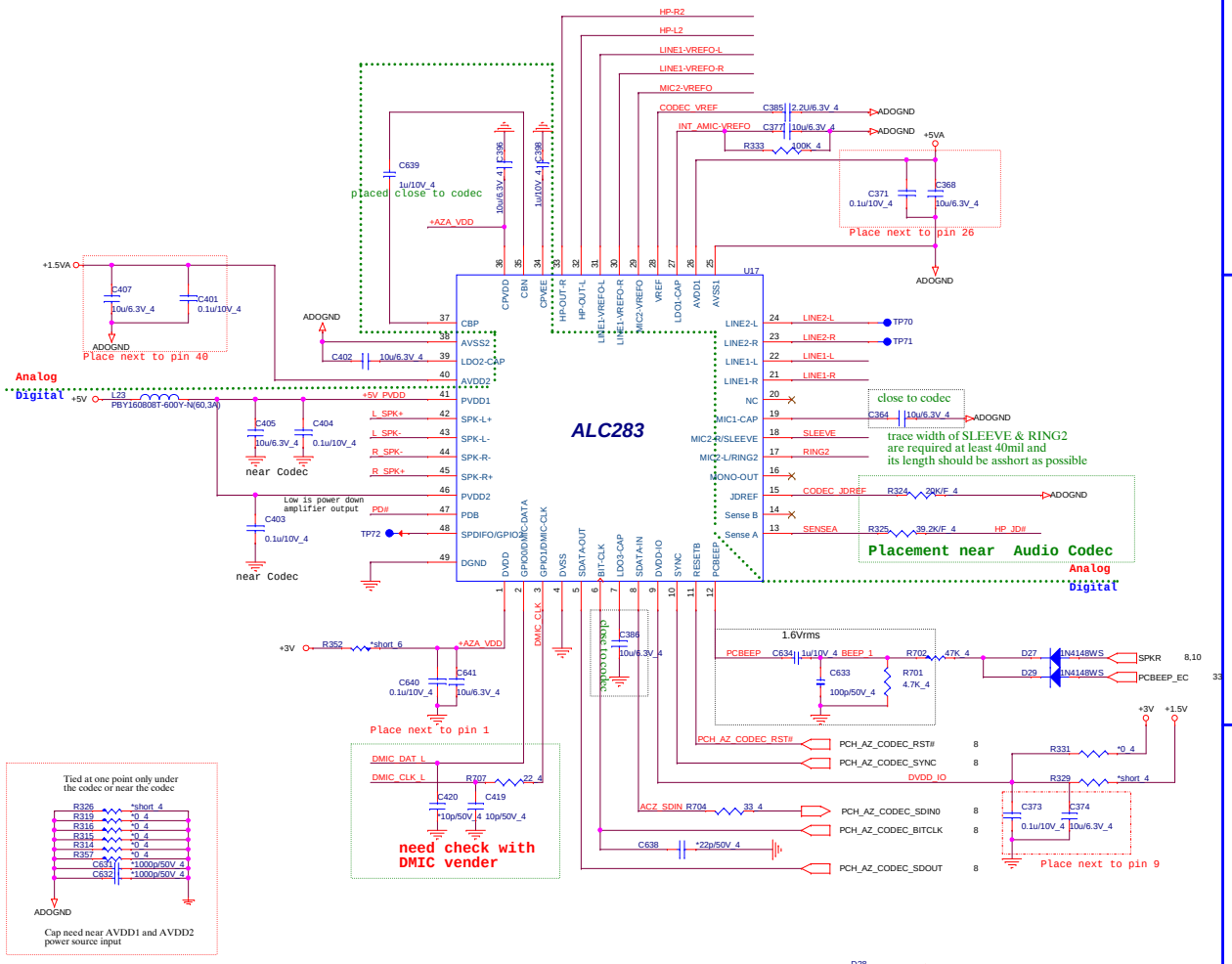
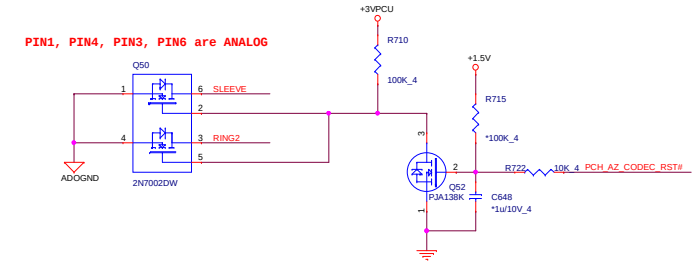
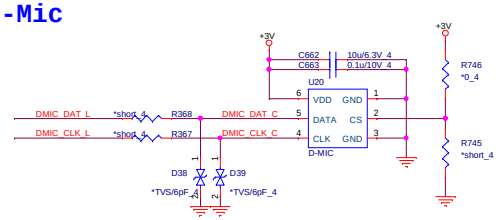
Codec(ADO)



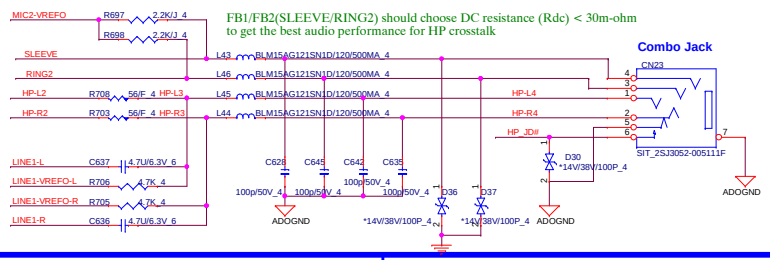
Grounding circuit(ADO)



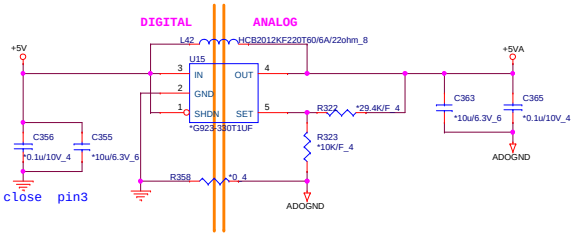
D-Mic



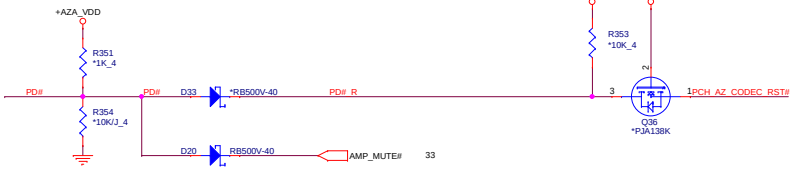
HEADPHONE/MIC/LINE combo (AMP)



Codec PWR 5V(ADO)



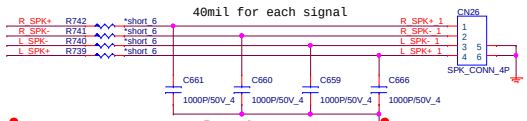
Mute(ADO)



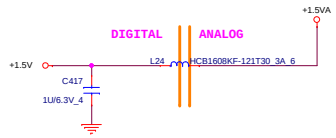
Level shift

Internal Speaker

Need Check P/N and F/P



Codec PWR 1.5V(ADO)



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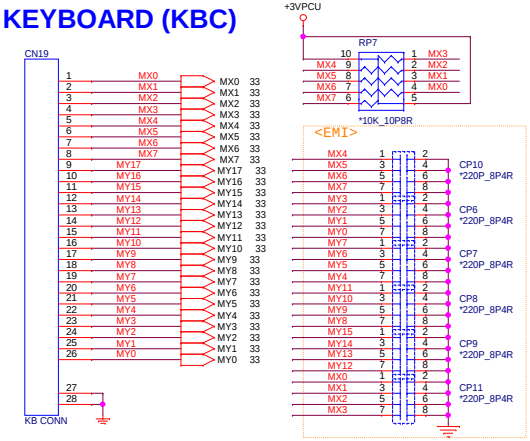
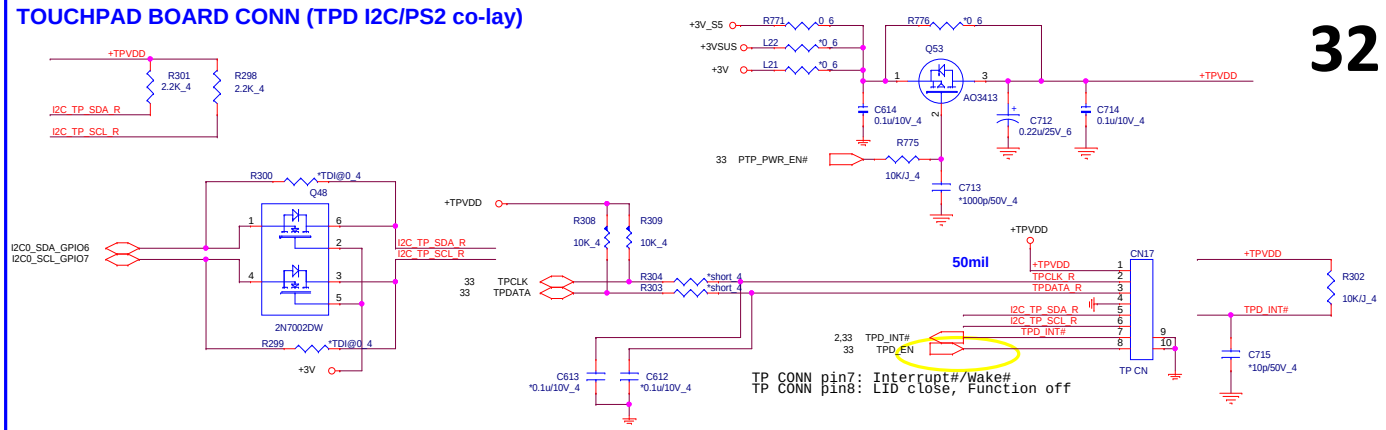
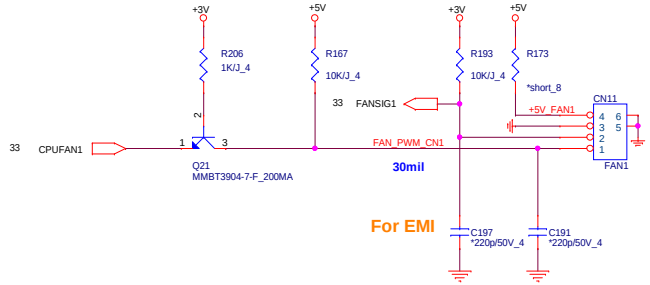
KEYBOARD (KBC)

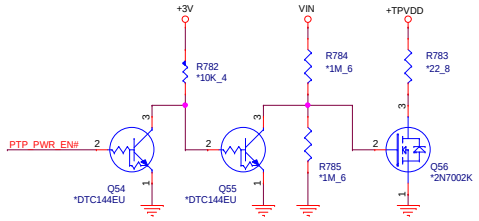


TOUCHPAD BOARD CONN (TPD I2C/PS2 co-lay)

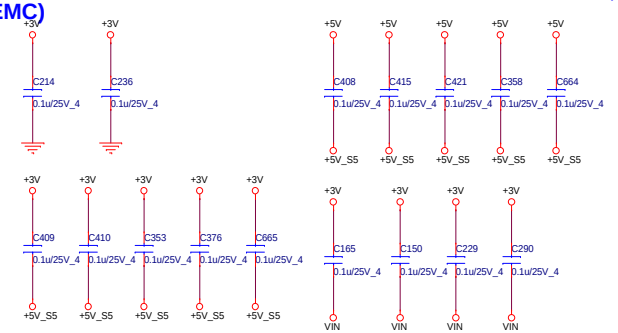


FAN1 For CPU (THM)

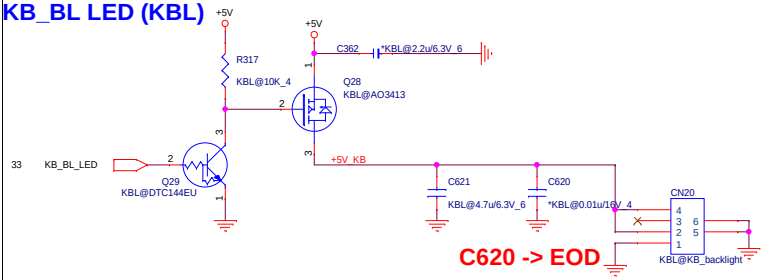




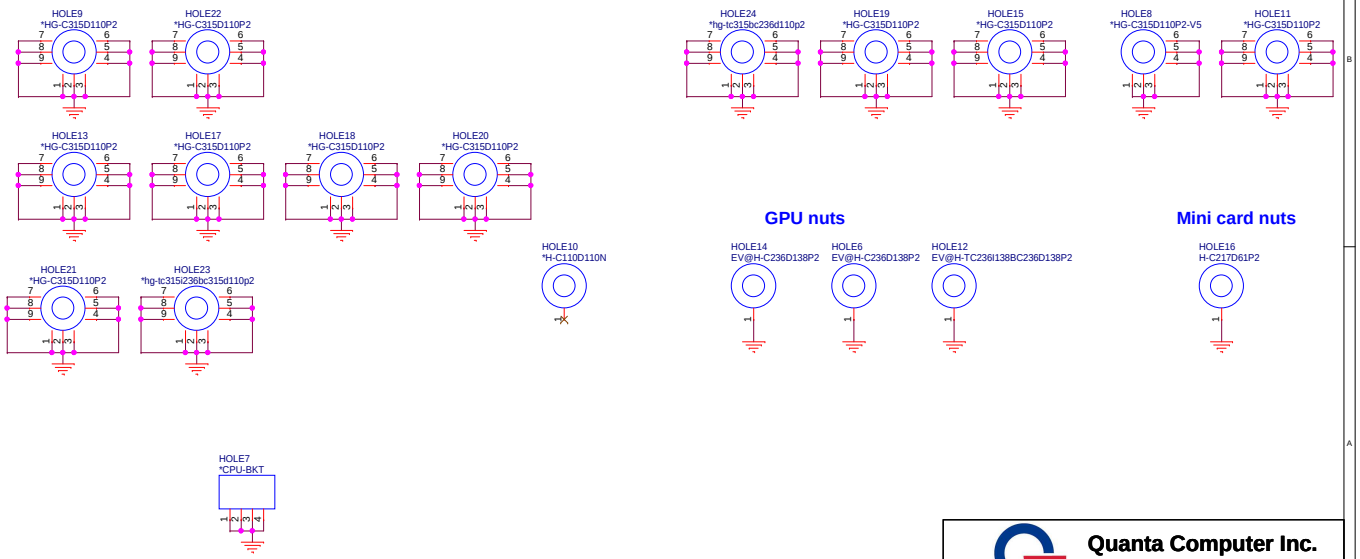
Stitch Caps (EMC)



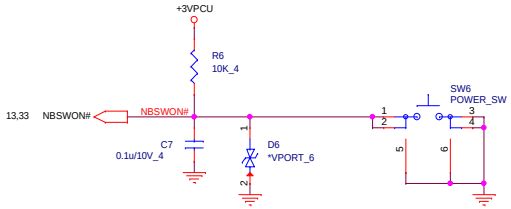
KB_BL LED (KBL)



NUT (OTH)



Power Switch. (FSW)



Quanta Computer Inc.

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Size	Document Number	Rev
	KB/TP/FAN	3A
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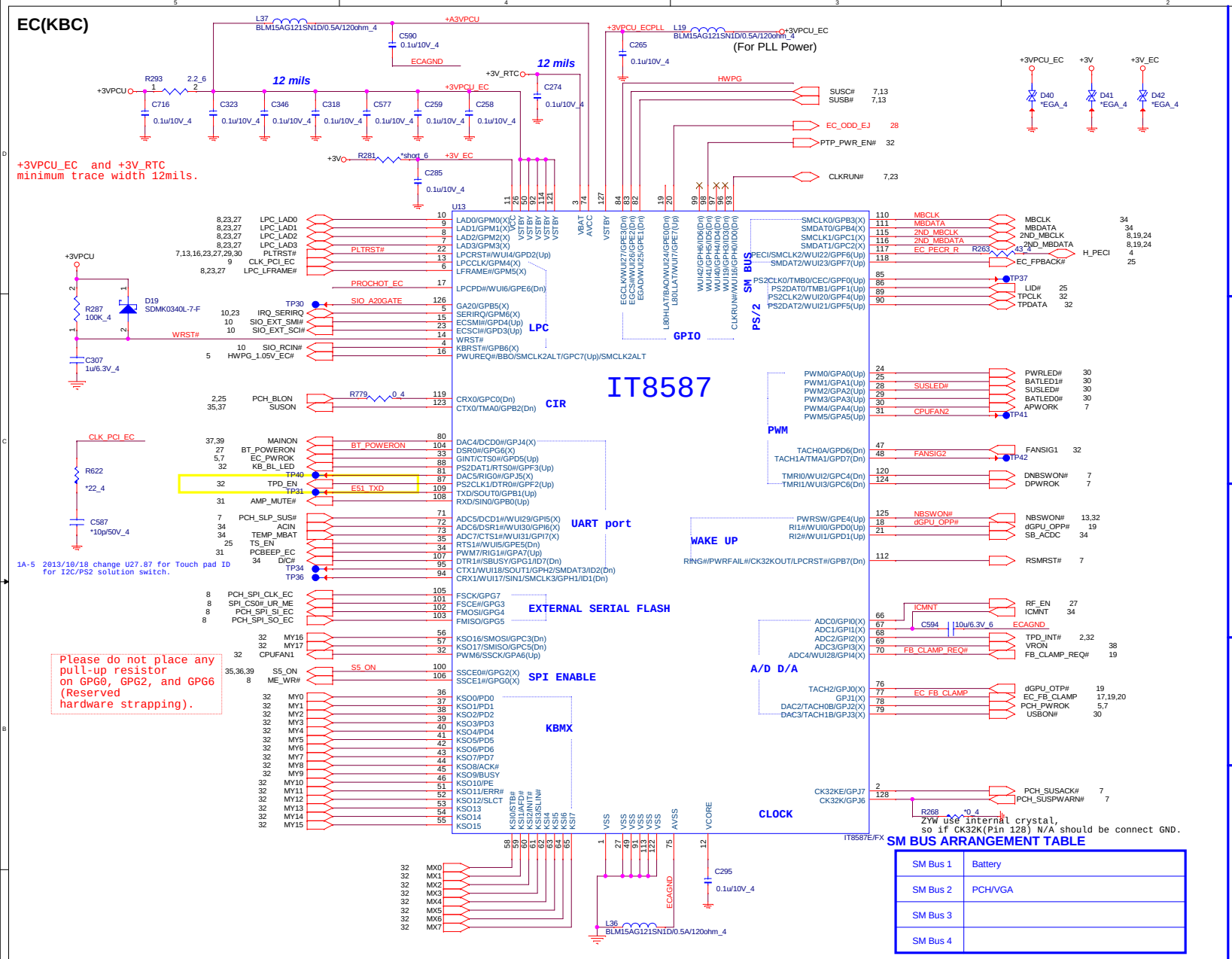
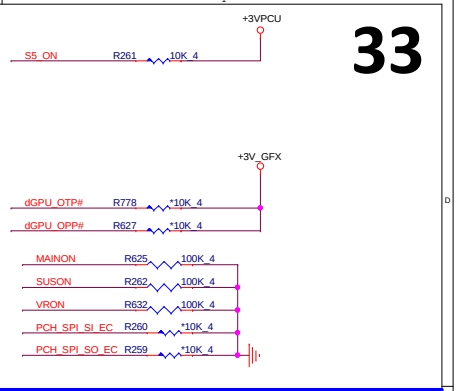
EC(KBC)

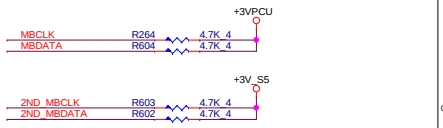


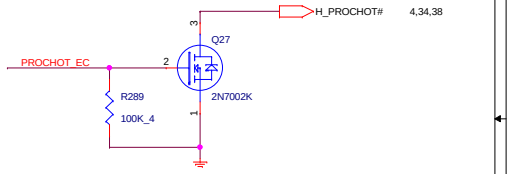
SM BUS ARRANGEMENT TABLE

SM Bus 1	Battery
SM Bus 2	PCH/VGA
SM Bus 3	
SM Bus 4	

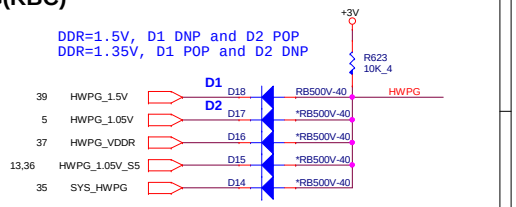


SM BUS PU(KBC)

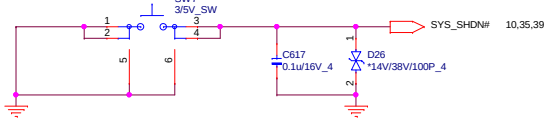




HWPG(KBC)



3/5VPCU reset switch (FSW)



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PROJECT : ZYW

Size	Document Number	Rev
	KBC IT8587	3A

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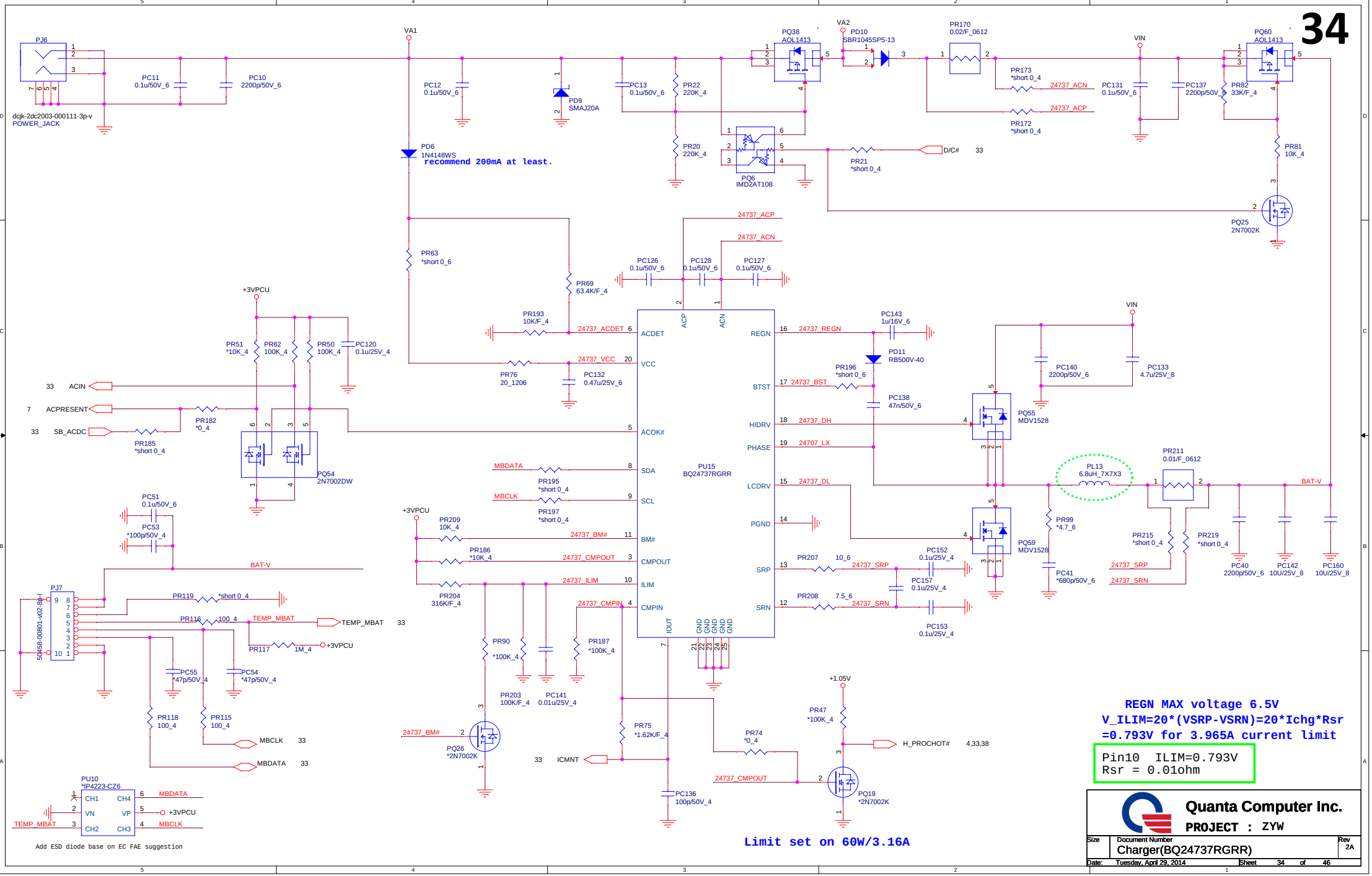
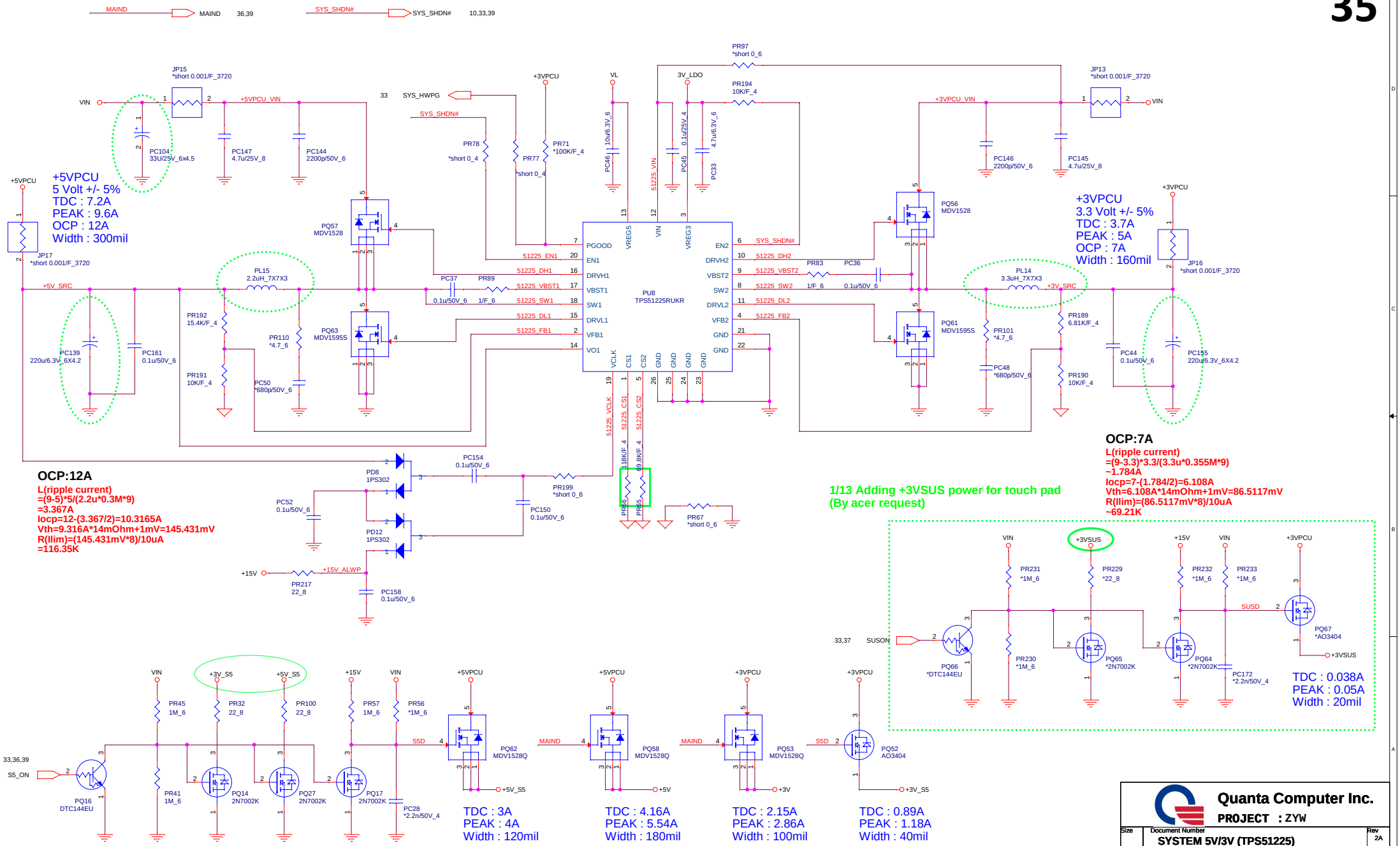


http://sualaptop365.edu.vn



Quanta Computer Inc.
PROJECT : ZYW
Size | Document Number: SYSTEM 5V/3V (TPS51225) | Rev 2A
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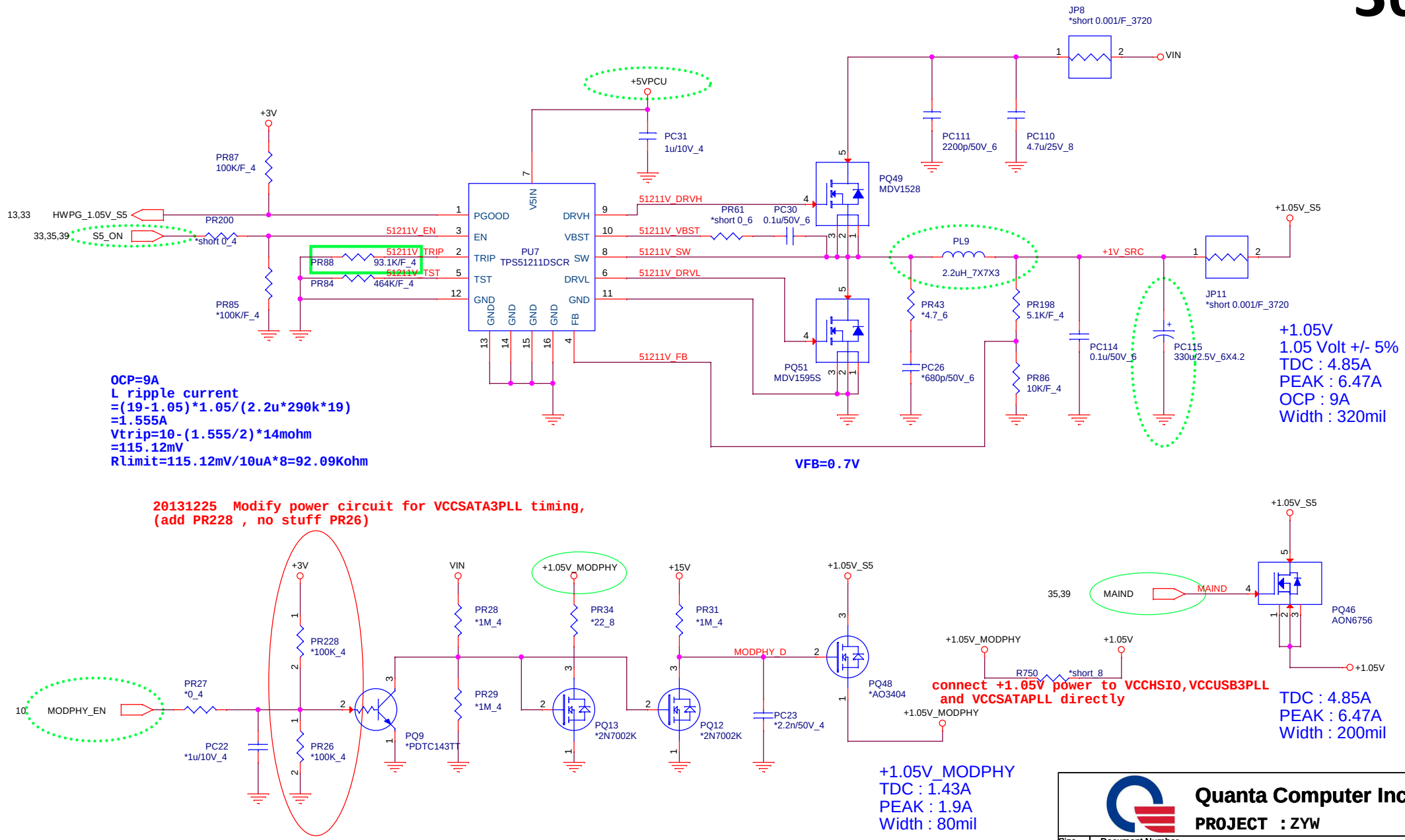

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PROJECT : ZYW

Size	Document Number	Rev
	+1.05V_S5 (TPS51211)	2A

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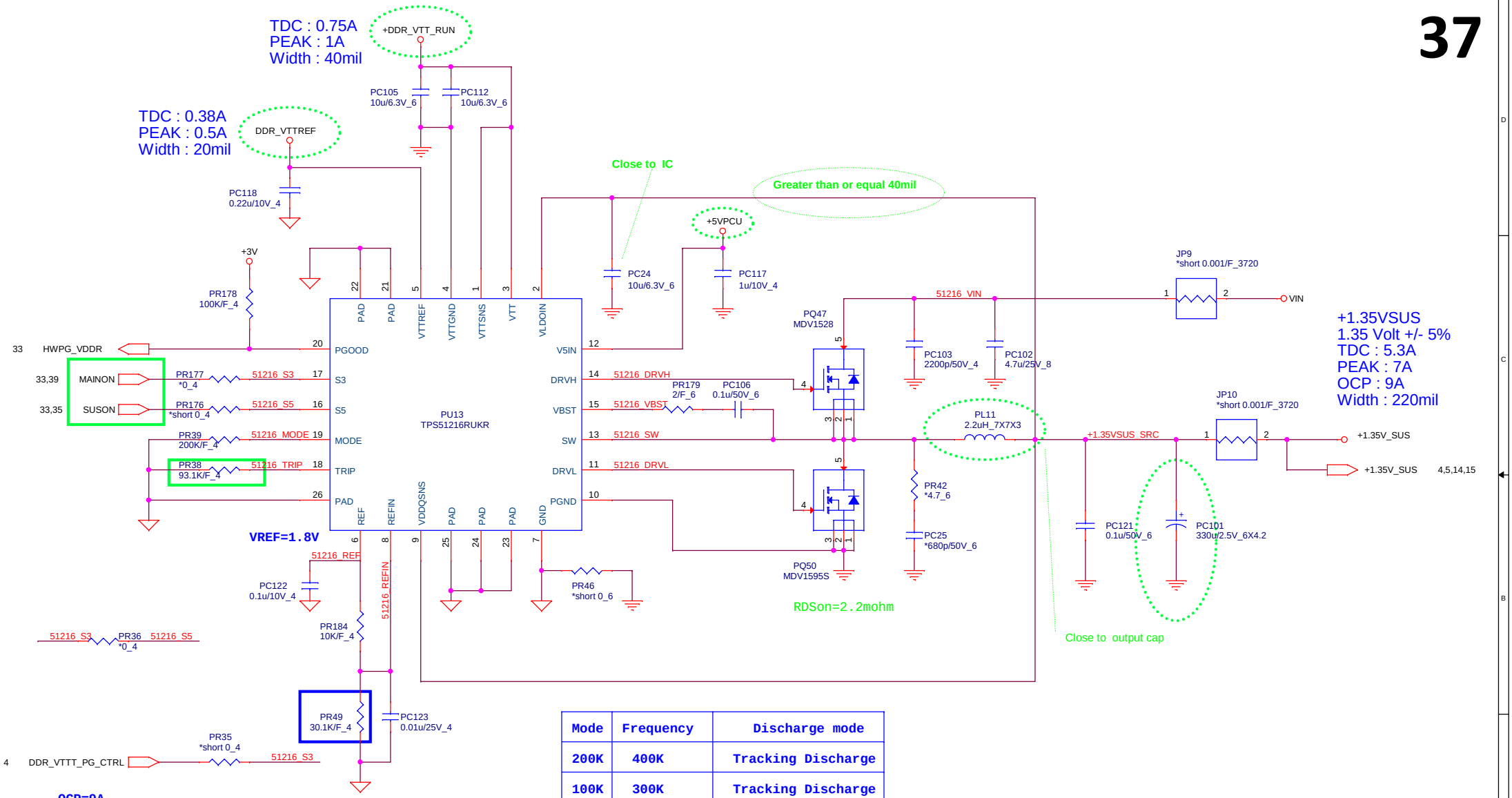

Mode	Frequency	Discharge mode
200K	400K	Tracking Discharge
100K	300K	Tracking Discharge

	S3	S5	+1.35VSUS	REF	VTT
S0	1	1	ON	ON	ON
S3 (mainon off)	0	1	ON	ON	OFF
S4/S5	0	0	OFF	OFF	OFF

OCP=9A
L ripple current
=(19-1.35)*1.35/(2.2u*400k*19)
=1.425A
Vtrip=9-(1.425/2)*14mohm
=116.024mV
Rlimit=116.024mV/10uA*8=92.82Kohm

DDR=1.35V
OCP=9A
PR84=10K/F_4
PR86=30.1K/F_4

Quanta Computer Inc.
PROJECT : ZYW

Size	Document Number	Rev
	DDR 1.35V(TPS51216)	2A

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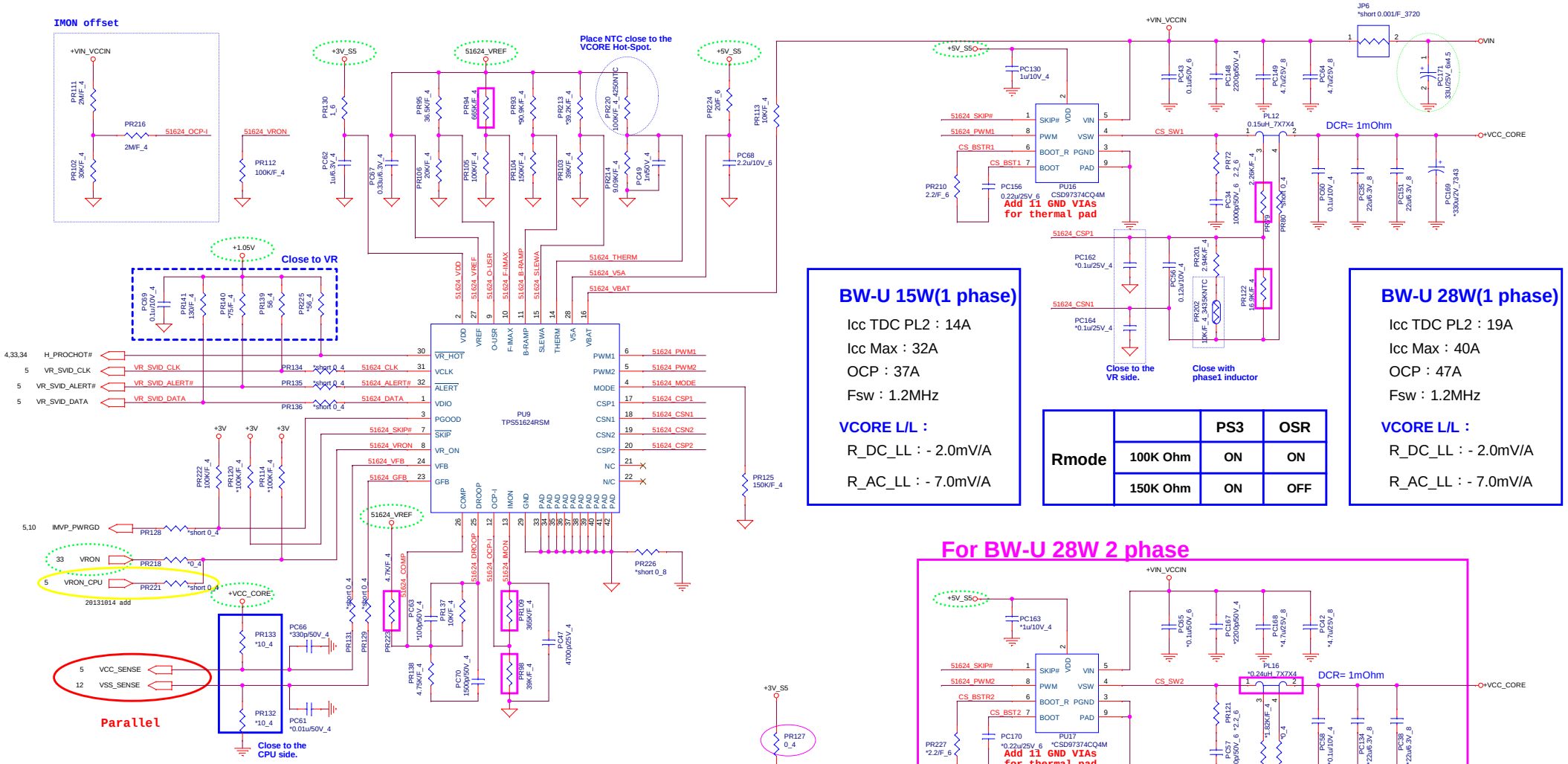


BW-U 15W(1 phase)

Icc TDC PL2：14A

Icc Max：32A

OCP：37A

Fsw：1.2MHz

VCORE L/L：

R_DC_LL：- 2.0mV/A

R_AC_LL：- 7.0mV/A

Rmode		PS3	OSR
	100K Ohm	ON	ON
	150K Ohm	ON	OFF

BW-U 28W(1 phase)

Icc TDC PL2：19A

Icc Max：40A

OCP：47A

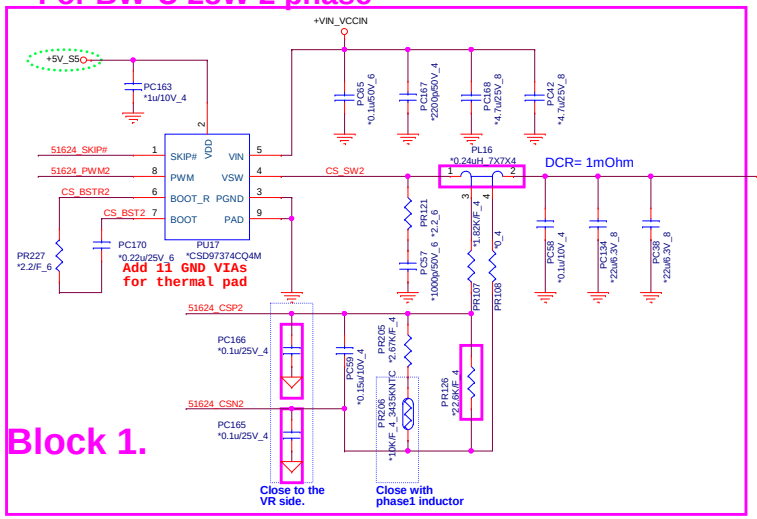
Fsw：1.2MHz

VCORE L/L：

R_DC_LL：- 2.0mV/A

R_AC_LL：- 7.0mV/A

For BW-U 28W 2 phase



BW-U 28W 1 phase

Location	Value
PR79	CS22212FB11
PR122	CS32262FB15
PR94	CS45232FB00
PR223	CS24752FB12
PR98	CS35622FB10
PR109	CS44122FB00

BW-U 28W 2 phase

Location	Value	Location	Value
PL12、PL16	0.24uH_7X7X4	PR105	56.2K/F_4
PR79	1.82K/F_4	PR223	2.37K/F_4
PR122、PR126	*22.6K/F_4	PR138	10K/F_4
PR201	2.67K/F_4	PR109	150K/F_4
PC144	0.15u/10V_4	PR123、PR127	*0_4
PR94	294K/F_4	PC162、PC164 PC165、PC166	*0.1u/25V_4
Block 1.	Stuff		

Quanta Computer Inc.

PROJECT : ZYW

Size | Document Number: +VCCIN(TPS51624) | Rev 2A

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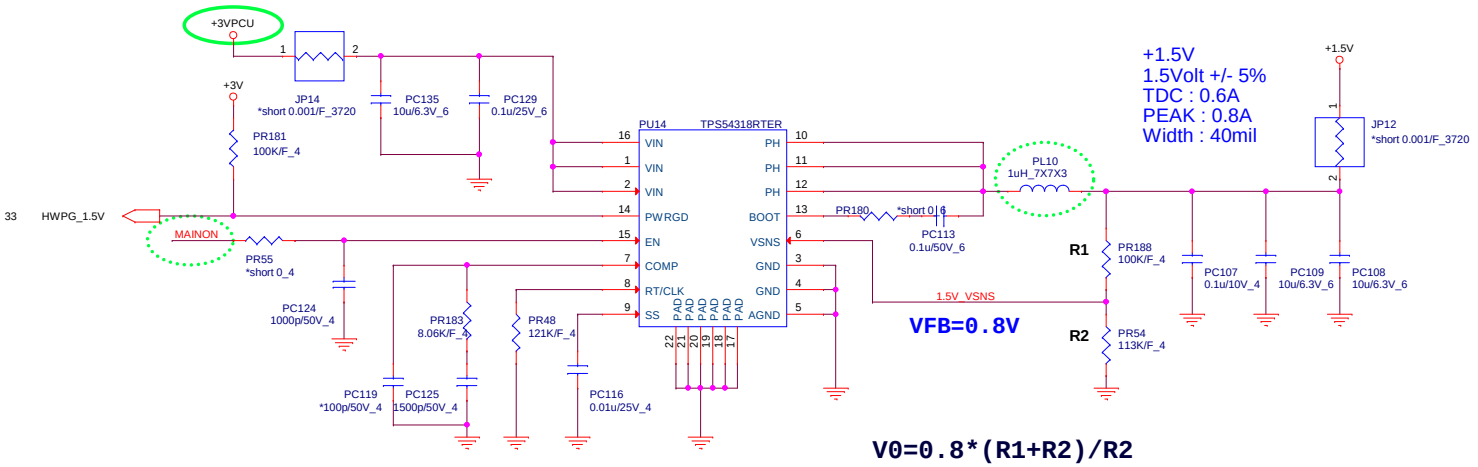


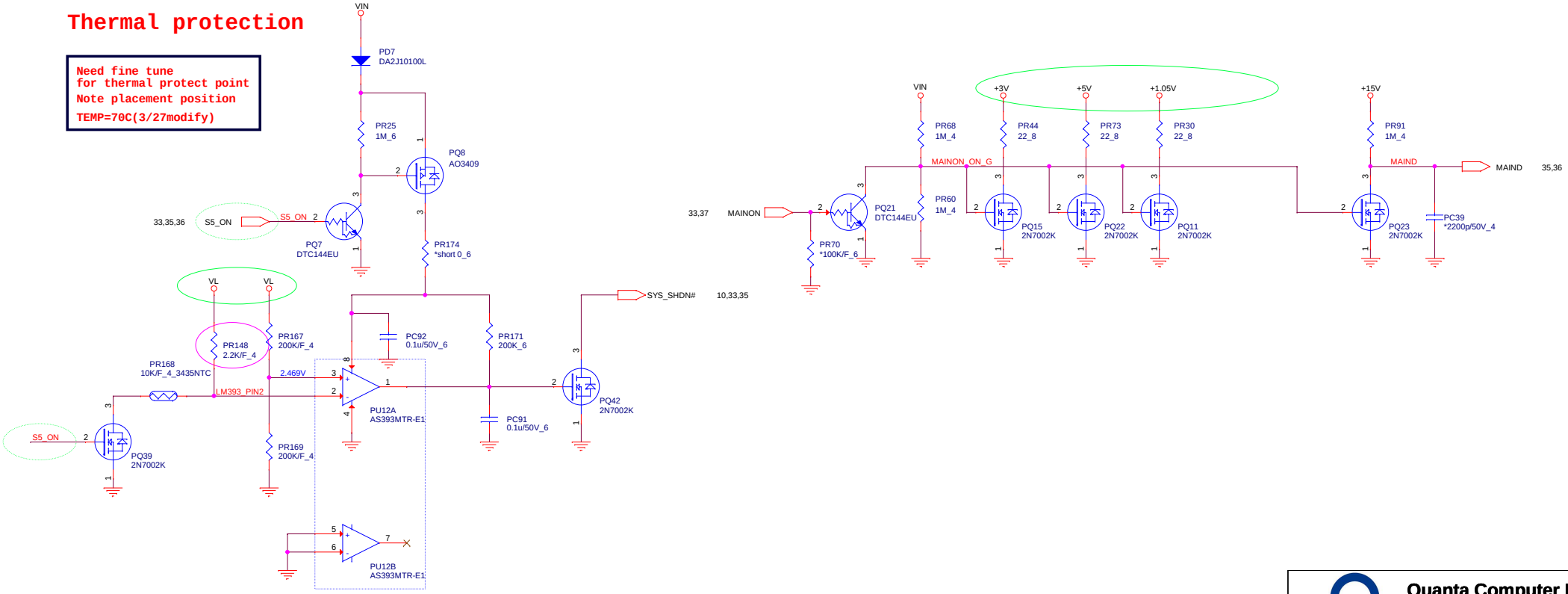
+1.5V
1.5Volt +/- 5%
TDC : 0.6A
PEAK : 0.8A
Width : 40mil

VFB=0.8V

V0=0.8*(R1+R2)/R2

Thermal protection

Need fine tune
for thermal protect point
Note placement position
TEMP=70C(3/27modify)



For EC control thermal protection (output 3.3V)

Quanta Computer Inc.
PROJECT : ZYW

Size	Document Number	Rev
	+1.5V/Thermal Protect	2A

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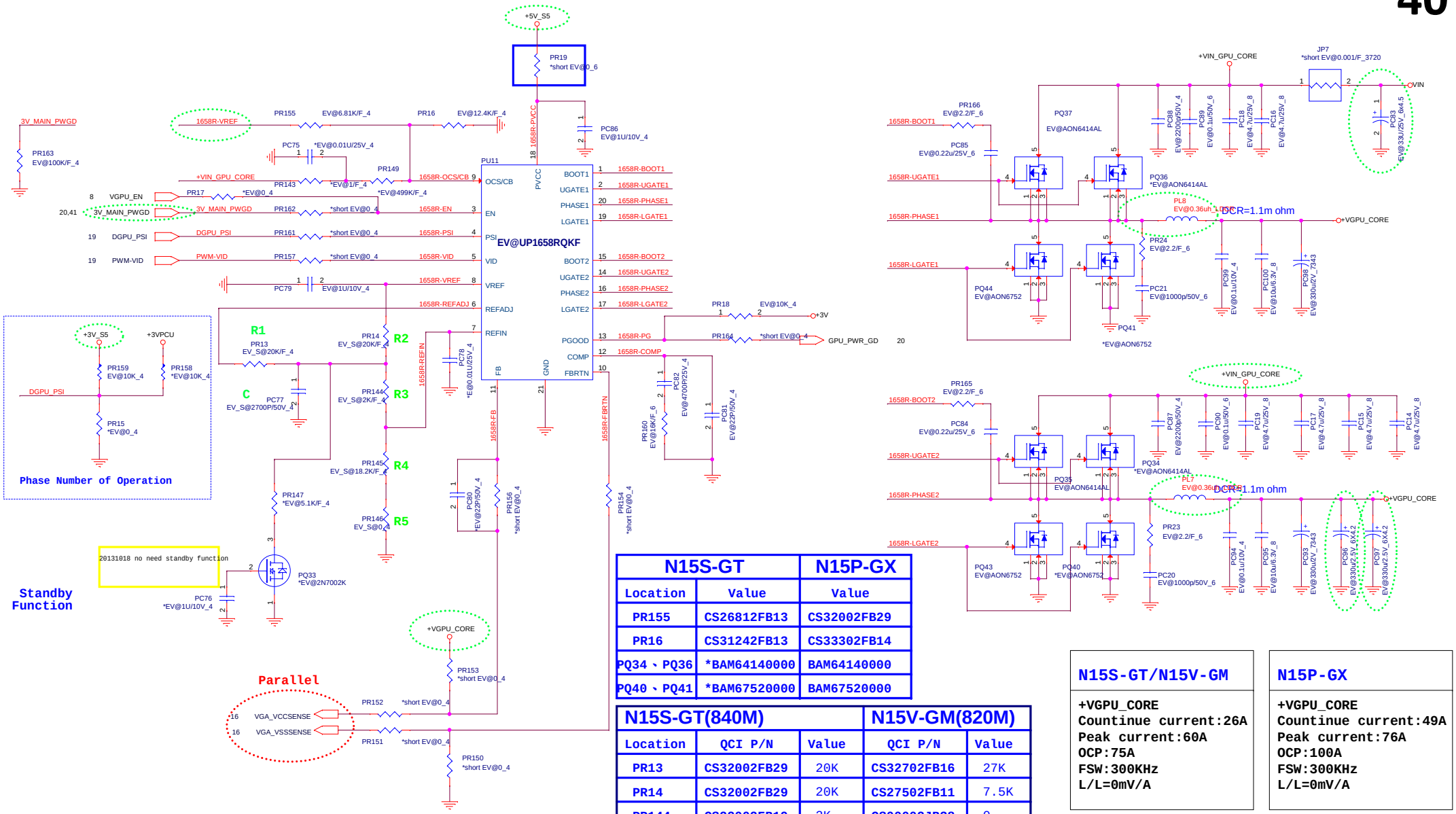

N15S-GT		N15P-GX
Location	Value	Value
PR155	CS26812FB13	CS32002FB29
PR16	CS31242FB13	CS33302FB14
PQ34、PQ36	*BAM64140000	BAM64140000
PQ40、PQ41	*BAM67520000	BAM67520000

N15S-GT(840M)			N15V-GM(820M)	
Location	QCI P/N	Value	QCI P/N	Value
PR13	CS32002FB29	20K	CS32702FB16	27K
PR14	CS32002FB29	20K	CS27502FB11	7.5K
PR144	CS22002FB19	2K	CS00002JB38	0
PR145	CS31822FB16	18K	CS26202FB17	6.2K
PR146	CS00002JB38	0	CS21742FB00	1.74K
PC77	CH22706KB14	2.7N	CH25604KB18	5.6N

N15S-GT/N15V-GM

+VGPU_CORE
Countinue current:26A
Peak current:60A
OCP:75A
FSW:300KHz
L/L=0mV/A

N15P-GX

+VGPU_CORE
Countinue current:49A
Peak current:76A
OCP:100A
FSW:300KHz
L/L=0mV/A

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Size	Document Number	Rev
	+VGPU_CORE(UP1642PQAG)	2A

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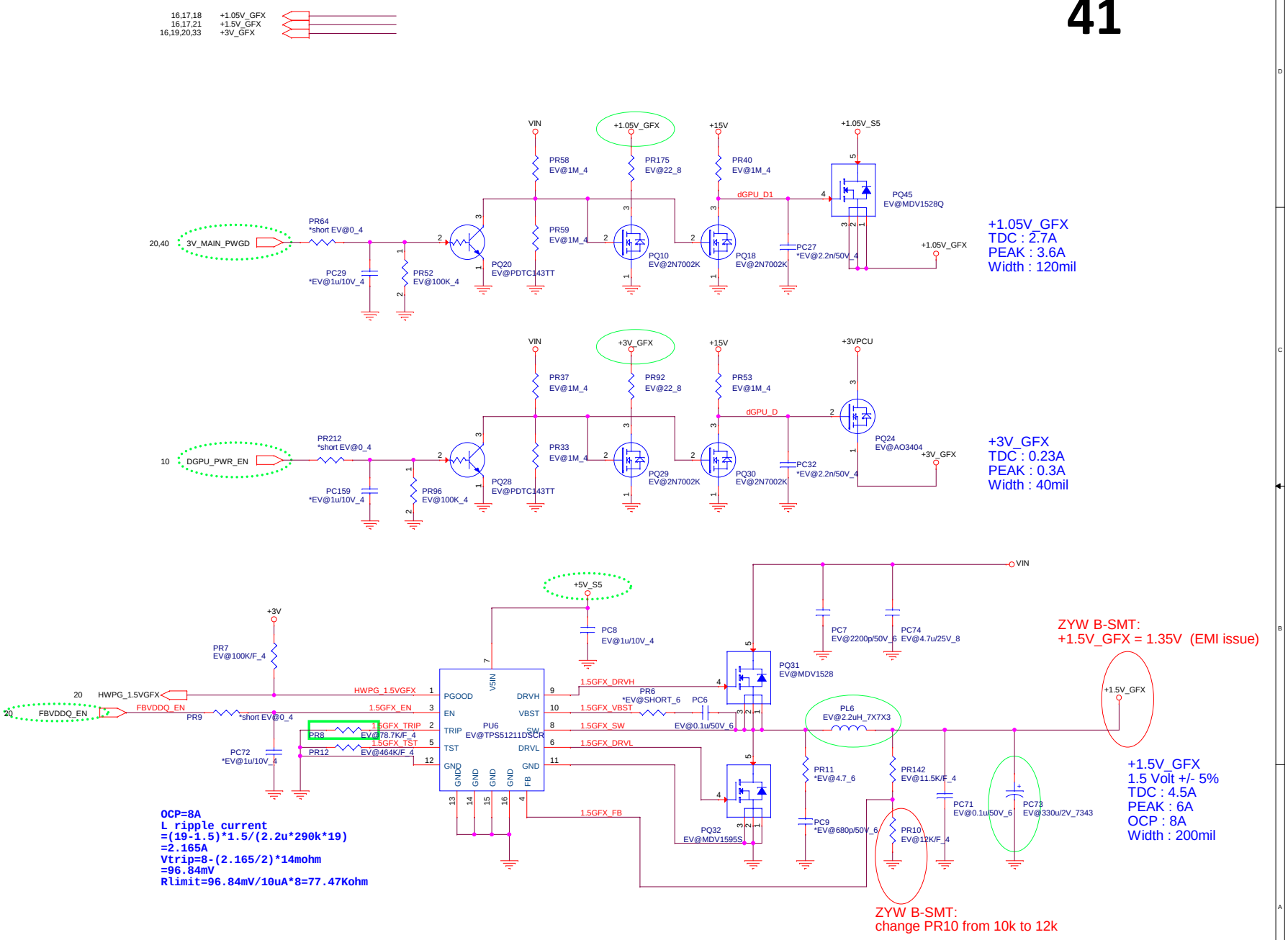

Quanta Computer Inc.

PROJECT : ZYW

Size	Document Number	Rev
	+1.5V_GFX/+1.05V_GFX/+3V_GFX	2A

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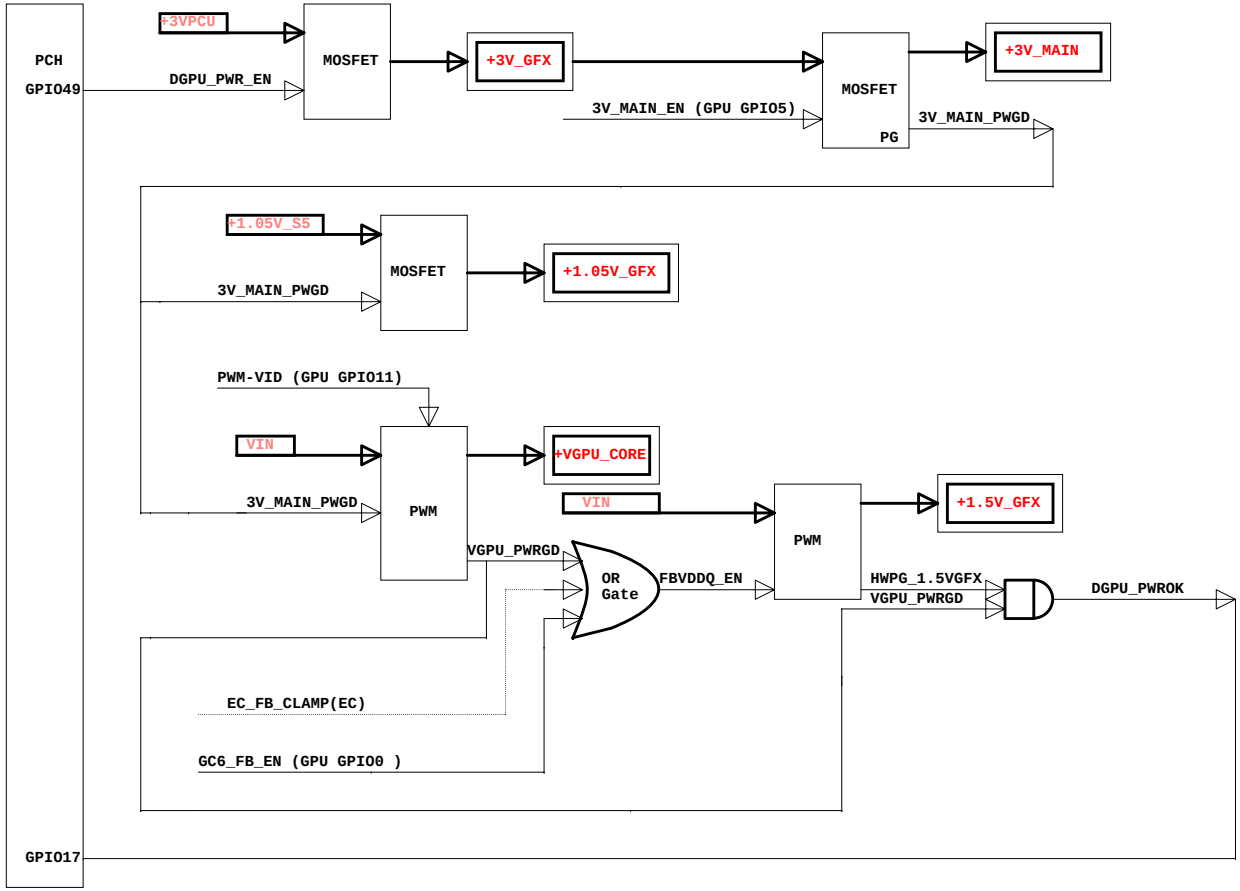
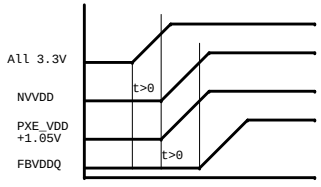
VGA power up sequence

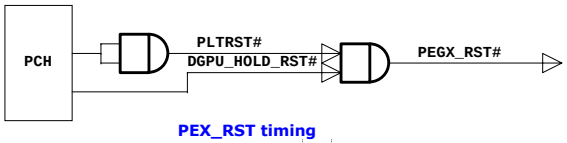




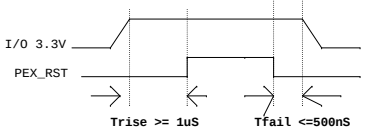
N15x Power on sequance

Notes: -All 3.3V includes all rails powered at 3.3V
-PEX_VDD 1.05V inculdes all rails that are shared

VGA Reset



PEX_RST timing



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Size	Document Number: GPU PWR CRL	Rev 3A
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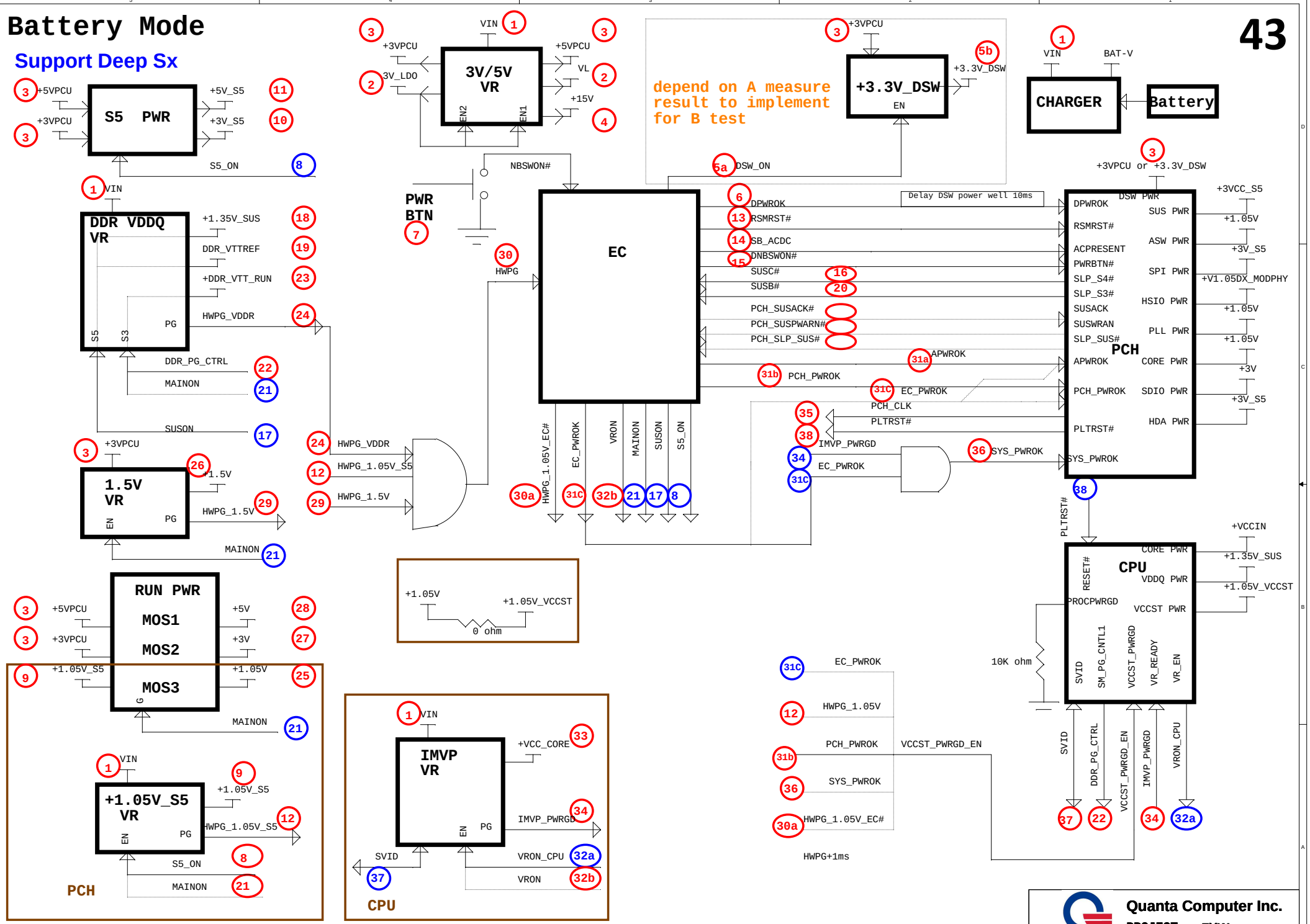
Battery Mode

Support Deep Sx



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Size	Document Number	Rev
	Power Sequence	3A

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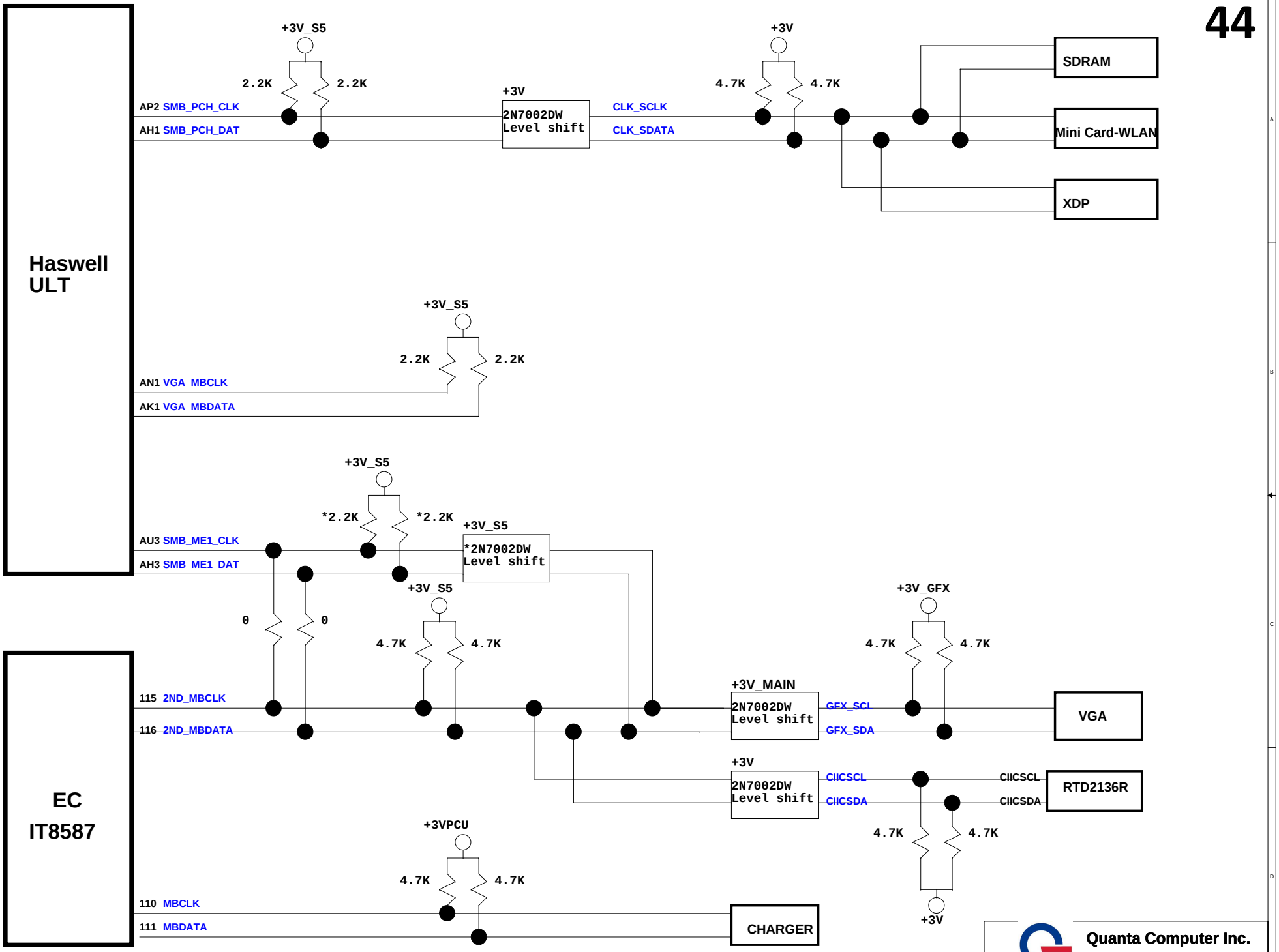

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Size	Document Number	Rev
	Block Diagram	3A

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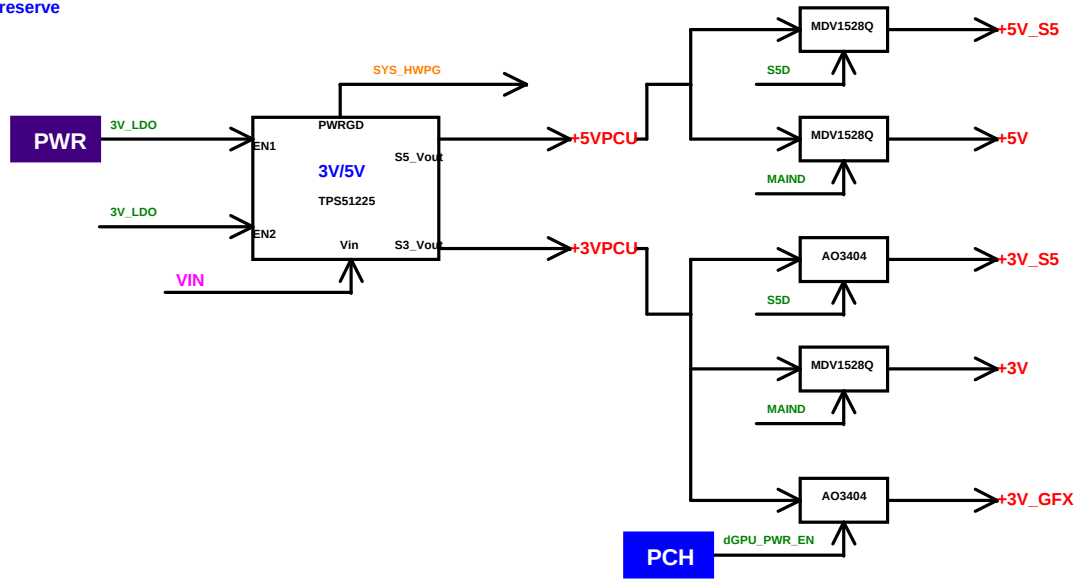
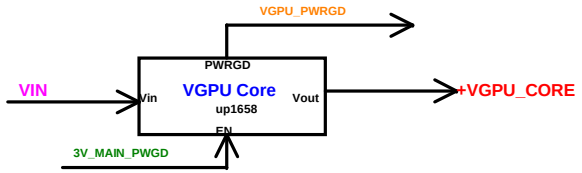
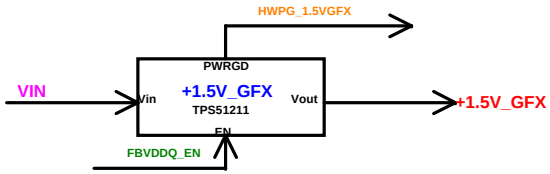
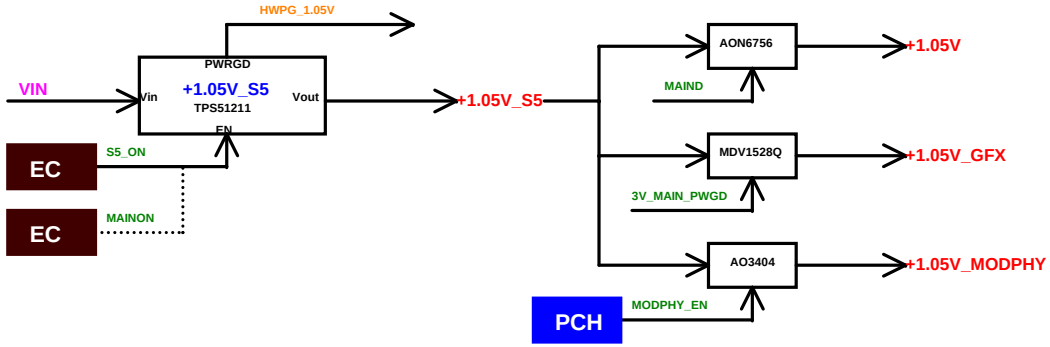
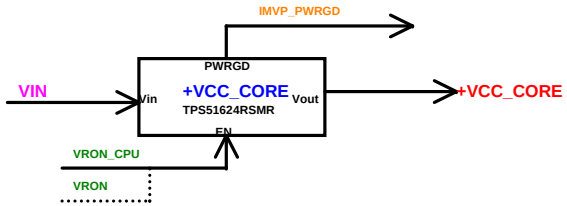
實線表defult
虛線表reserve

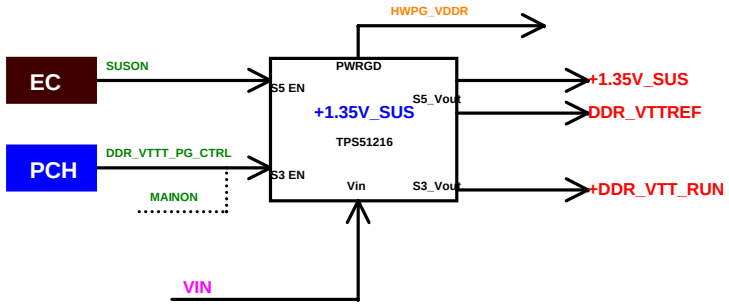


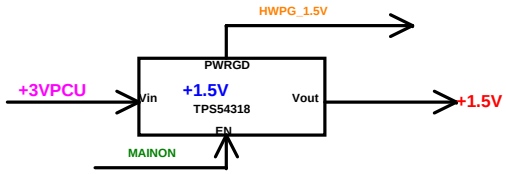












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Size	Document Number	Rev
	ULT PWR CONTROL	3A

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